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SEPT 1

Issue 18/2006

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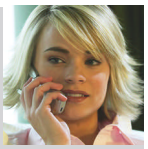
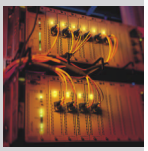
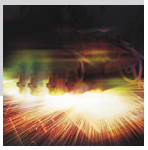
For the past 40 years, we've been inventing the future.







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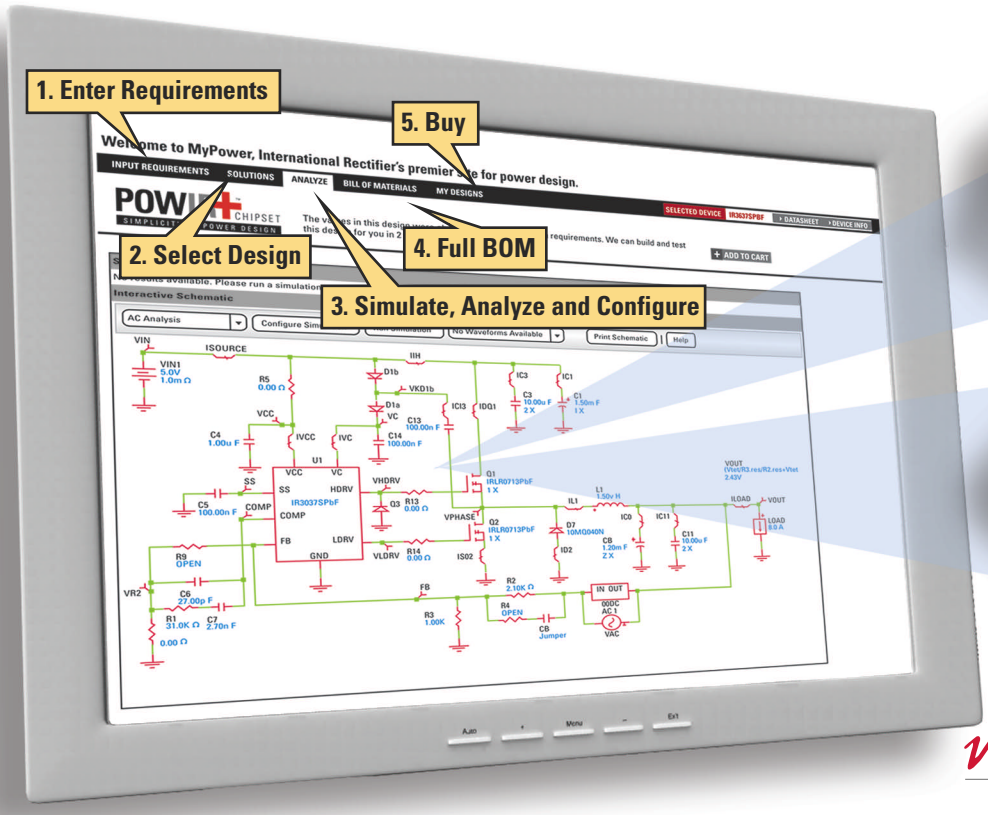
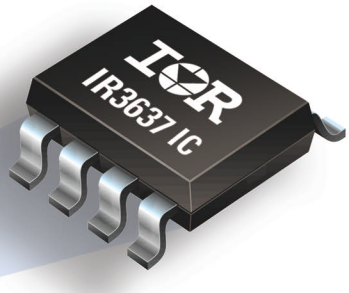
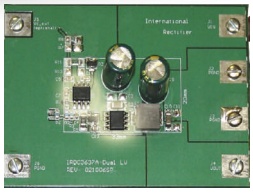




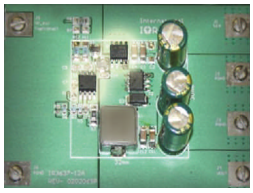
myPOWER online design

IRPP3637-06A



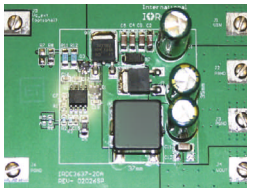
5V$_{in}$ / 1.25V$_{out}$
@ 6A & 600kHz ~1.0in^2

IRPP3637-12A



12V$_{in}$ / 1.8V$_{out}$
@ 12A & 400kHz ~1.5in^2

IRPP3637-18A



12V$_{in}$ / 3.3V$_{out}$
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Part Number	Input Voltage	Output Voltage	Output Current	Swithcing Frequency	Power Semi BOM	Delivery Time	Comments
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IRPP3637-12A	12V	1.8V	12A	400kHz	IR3637S, IRF7823, IRF7832Z		
IRPP3637-18A	12V	3.3V	18A	400kHz	IR3637S, IRLR8713, IRLR7843		
IRPP3637-06AC	3.0V to 13.2V	0.8V to 5.0V	Up to 6A	400kHz or 600kHz	Various	1-2 Wks	Customizable Ref Design BOM configurable on-line. Operating range defined is NOT possible with one BOM
IRPP3637-12AC			Up to 12A		Various		
IRPP3637-18AC			Up to 18A		Various		

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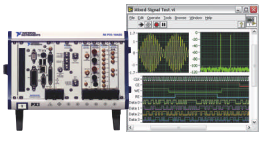

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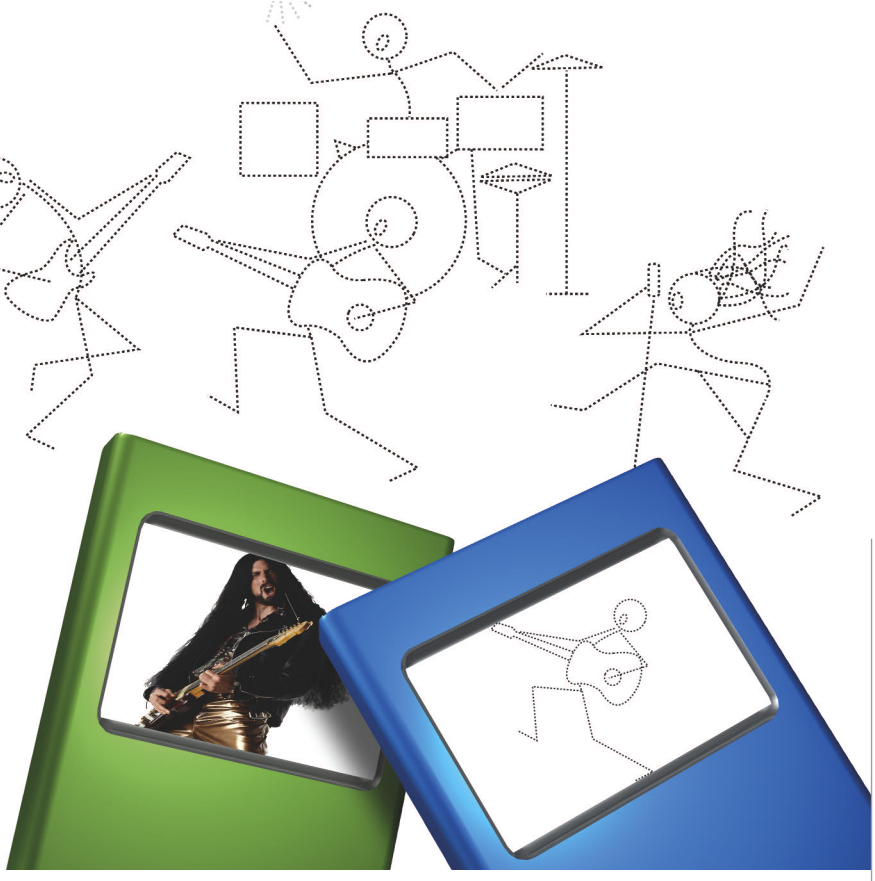

The right video architecture can make all the difference

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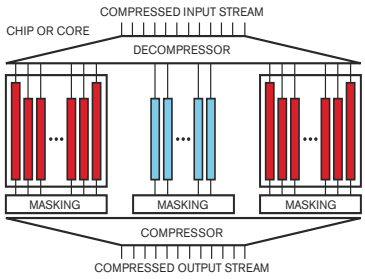
by Ron Wilson, Executive Editor

Clash of the wireless-USB standards

37 Wireless USB is poised to enter the market. Understanding the differences between the two leading approaches will help developers choose the right one for their application.

by Richard A Quinnell, Contributing Technical Editor



An overview of on-chip compression architectures

61 Data-compression techniques can help manage the escalating cost of test in nanometer designs.

by Brion Keller, Cadence Design Systems

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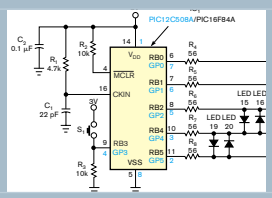

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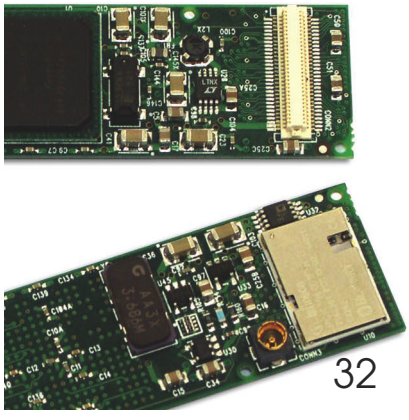

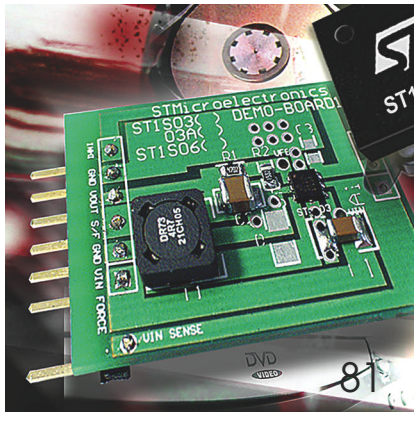

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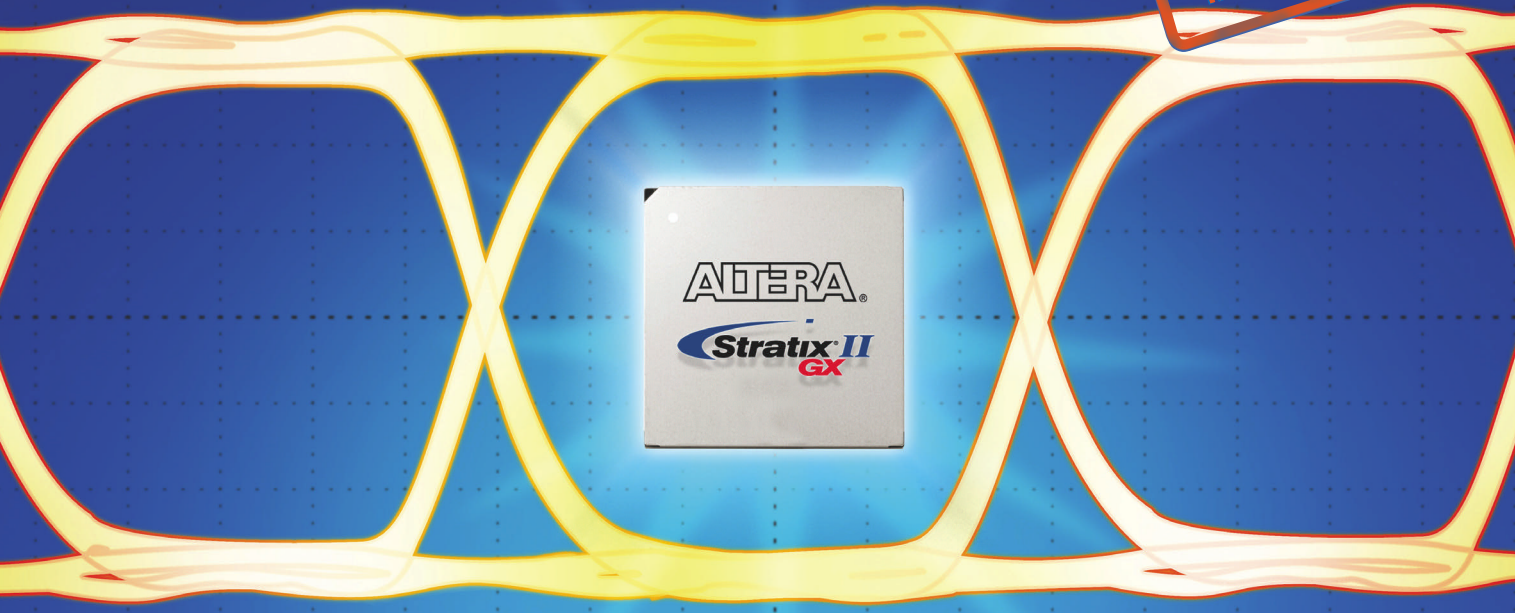

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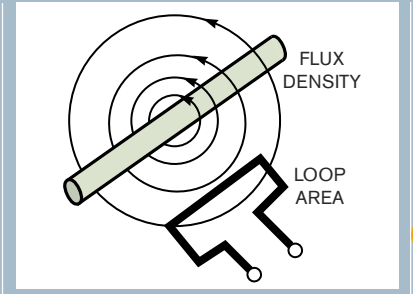

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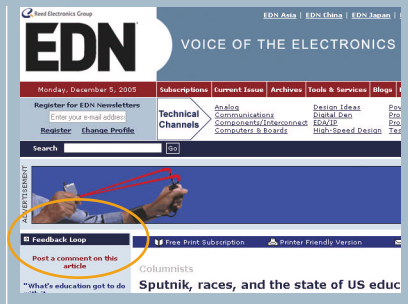

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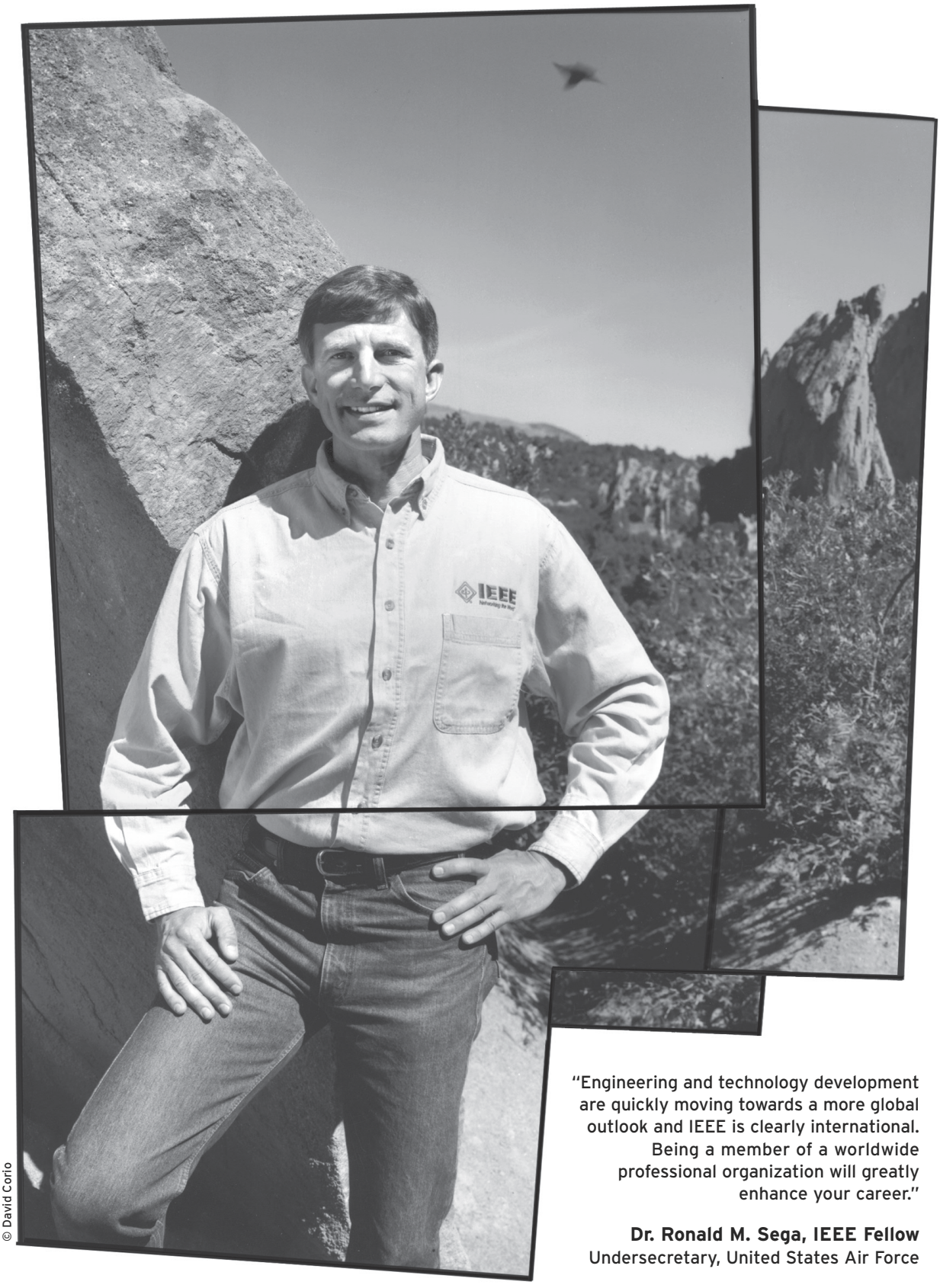

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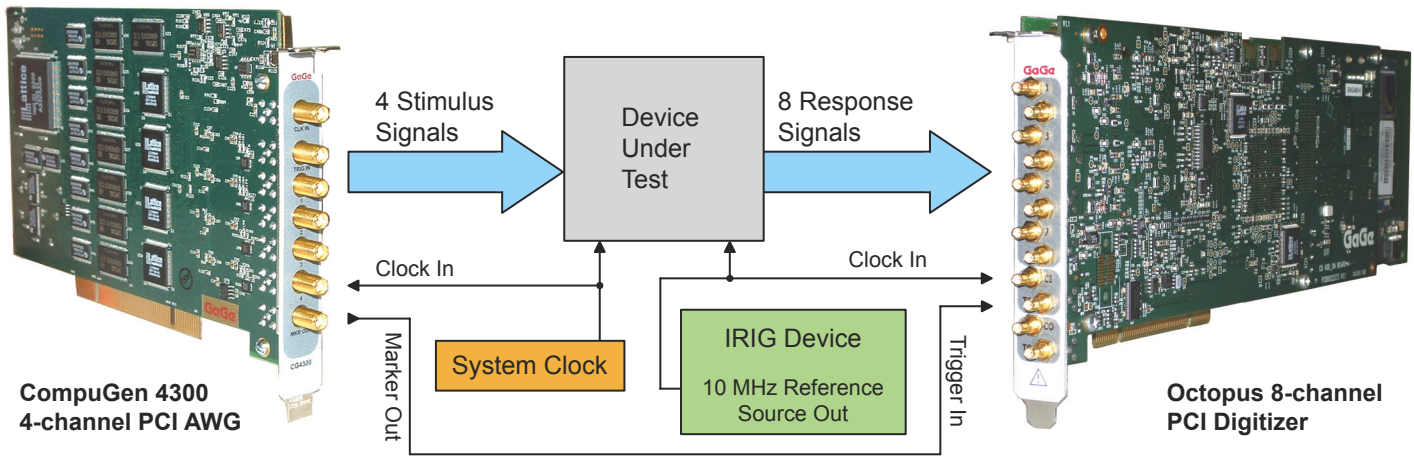

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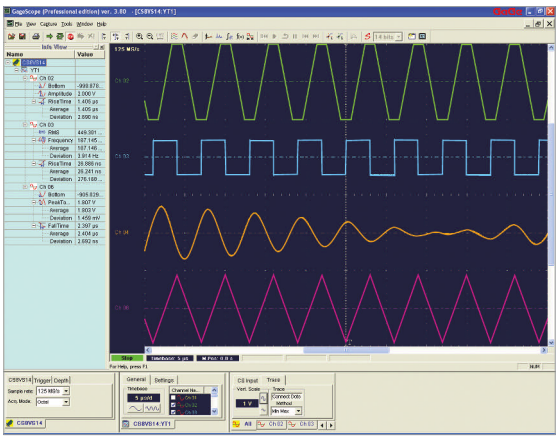

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BY MAURY WRIGHT, EDITOR IN CHIEF

Sportslike competition drives science and technology education

We in the trade press are asked daily to spread the word about everything from new products to "can't-miss" upcoming events or seminars. Our role as filters of information means that we say no most of the time. At the recent National Instruments Week conference, however, Dean Kamen, founder of DEKA Research and Development Corp (www.dekaresearch.com) and inventor of the Segway, pleaded for help in spreading the word about FIRST (For Inspiration and Recognition of Science and Technology, www.usfirst.org), the organization he founded in 1989. FIRST is an attempt to transform our culture and make science and technology as attractive to kids as sports and entertainment.

Kamen is a compelling speaker. He offered a disclaimer at the beginning of his talk suggesting that he was not an accomplished speaker. Don't believe it. All engineers should hear his thoughts on innovation. I'll share some of those thoughts in a future column. But here I'll stick to his thoughts on encouraging technical careers and the global race to develop a deep technical-talent pool. (See the **sidebar**, "Global friends or foes," at the Web version of this editorial at www.edn.com/060901ed1.)

On DEKA's home page, you'll find the following Kamen quote: "You have teenagers thinking that they are going to make millions as NBA stars when that's not realistic for even 1% of them. Becoming a scientist or engineer is." Kamen laments that kids aspire and work toward being sports heroes or entertainment celebrities. Meanwhile, he argues that scientists and engineers are almost completely responsible for the incredible standard of living that we enjoy today.

On kids' passion for sports, Kamen states, "They are all amazed that you can get the ball through the hoop 72% of the time ... They wouldn't want to fly in an airplane that landed 72% of the time." Kamen even attacks technology as a distraction. He says, "Kids would rather [be sitting] in front of that mind-numbing video game than designing it or building it or understanding it or improving it."

Through FIRST, Dean Kamen and his many partners are using a sports model to encourage kids to discover their inner engineer.

Through FIRST, Kamen and his many partners are using a sports model to encourage kids to discover their inner engineer. Kamen structured the FRC (FIRST Robotics Competition) like a high-school sports season. Teams get a kit of parts and a limited time to design and build a robot for competition. The first FRC took place in 1992 with the help of 23 sponsor companies and 28 competing teams.

Kamen claims that the competition was an immediate success with the participants and that the engineers who served as mentors liked it as much as the kids did. Those engineers remembered why they became engineers. Success and growth have led the final tournament to a venue at Walt Disney World, then to the Astrodome, and ultimately to the Georgia Dome. Now, regional competitions around the world feed the final competition. Moreover, this success led FIRST to create the FLL (FIRST Lego League) competition for middle-school kids and, more recently, the FVC (FIRST Vex Challenge), which is a more affordable competition than the FRC. In 2005, 1133 teams competed in the FRC, 7500 teams competed in the FLL, and 300 teams took part in the new FVC.

Despite the success, Kamen thinks FIRST needs to reach out to many more kids. The cause is noble, so I'm happy to spread the word. If you and your company are not involved in FIRST, at least take a look at the organization. You might find it very fulfilling, and you might help to ensure continued innovation wherever you live. EDN

You can reach me at 1-858-748-6785 or mgwright@edn.com.

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Up to 1.8 A	Up to 2.3 A	Up to 2.0 A	Up to 5.0 A	Up to 4.8 A
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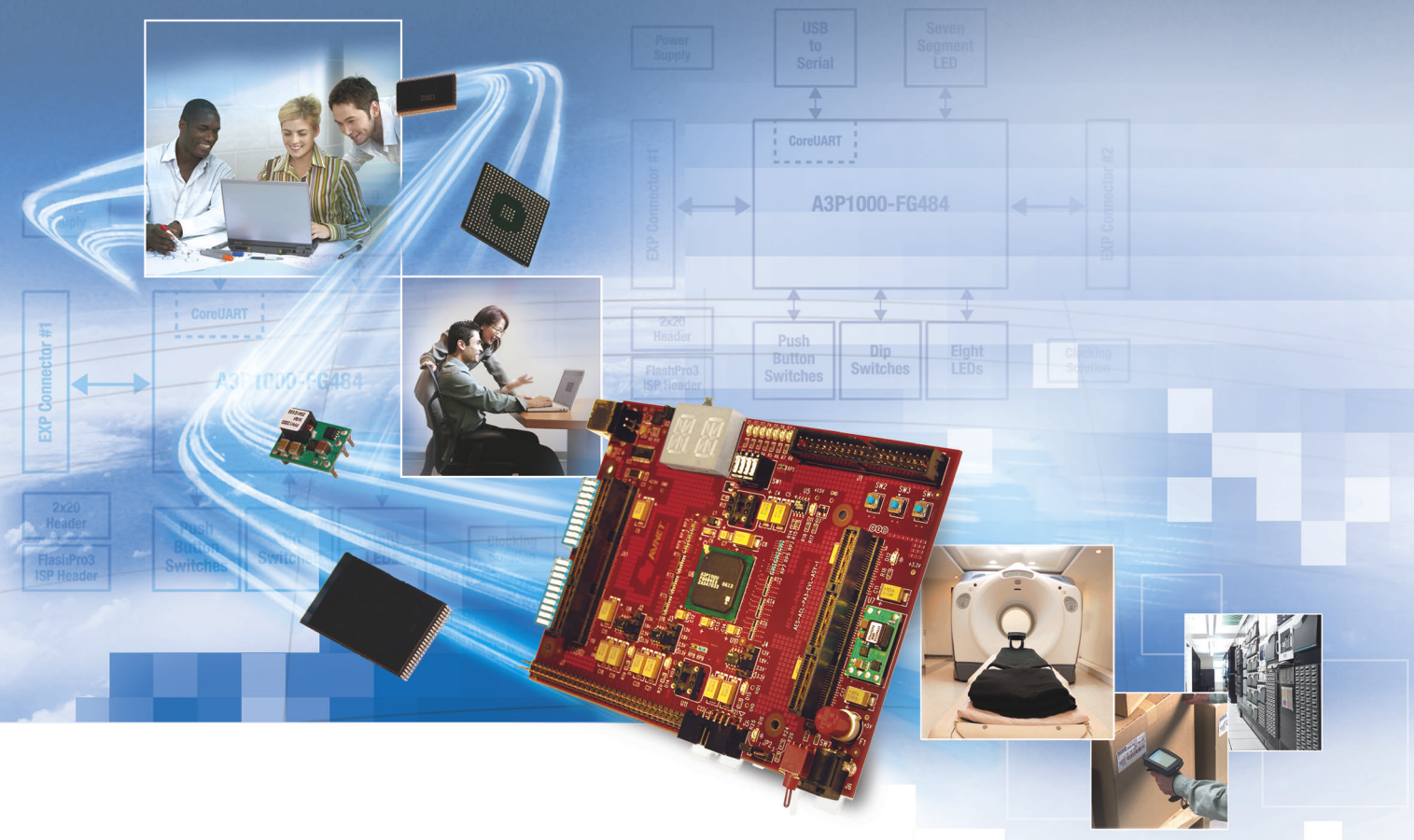

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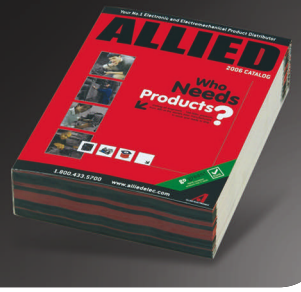

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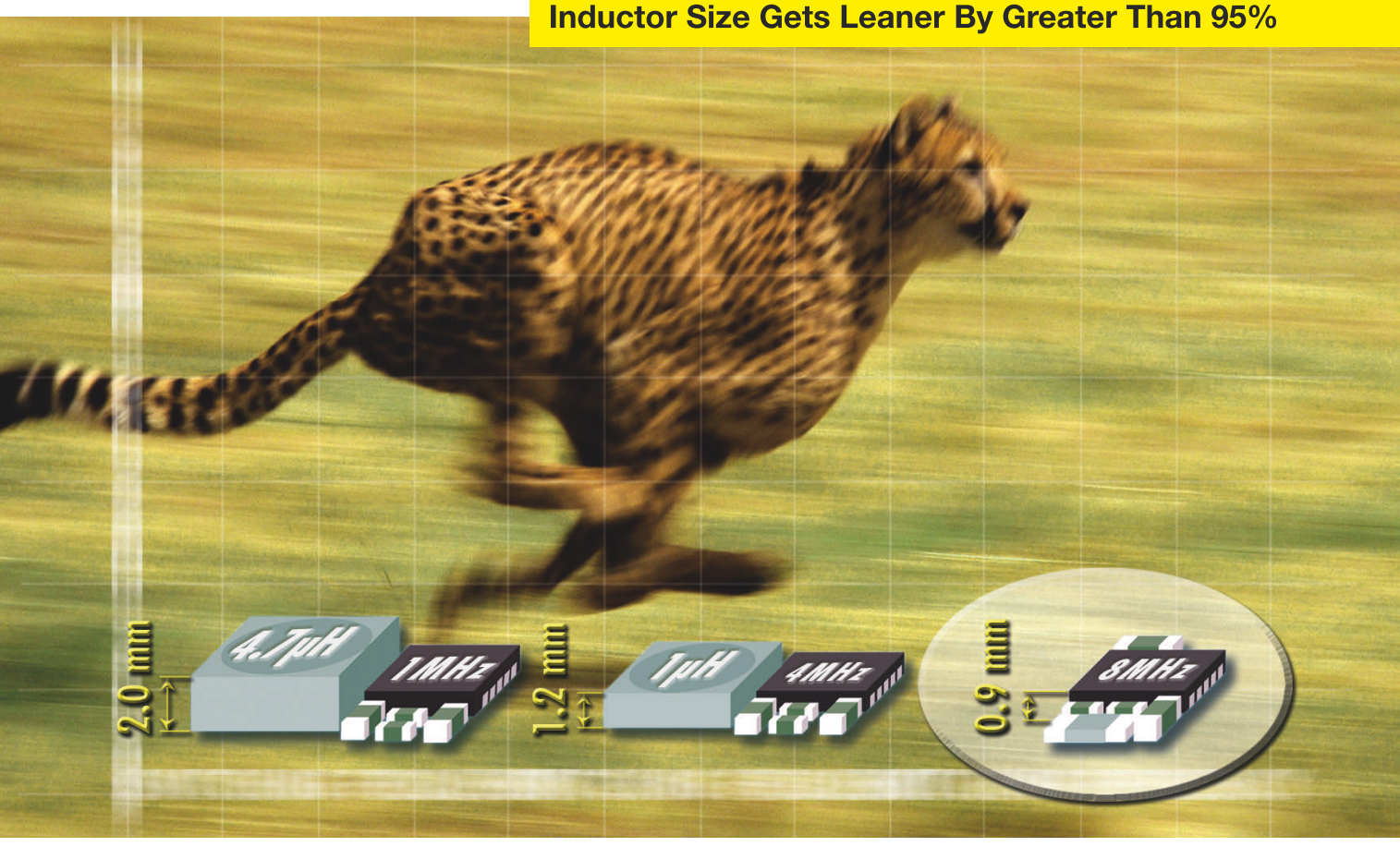

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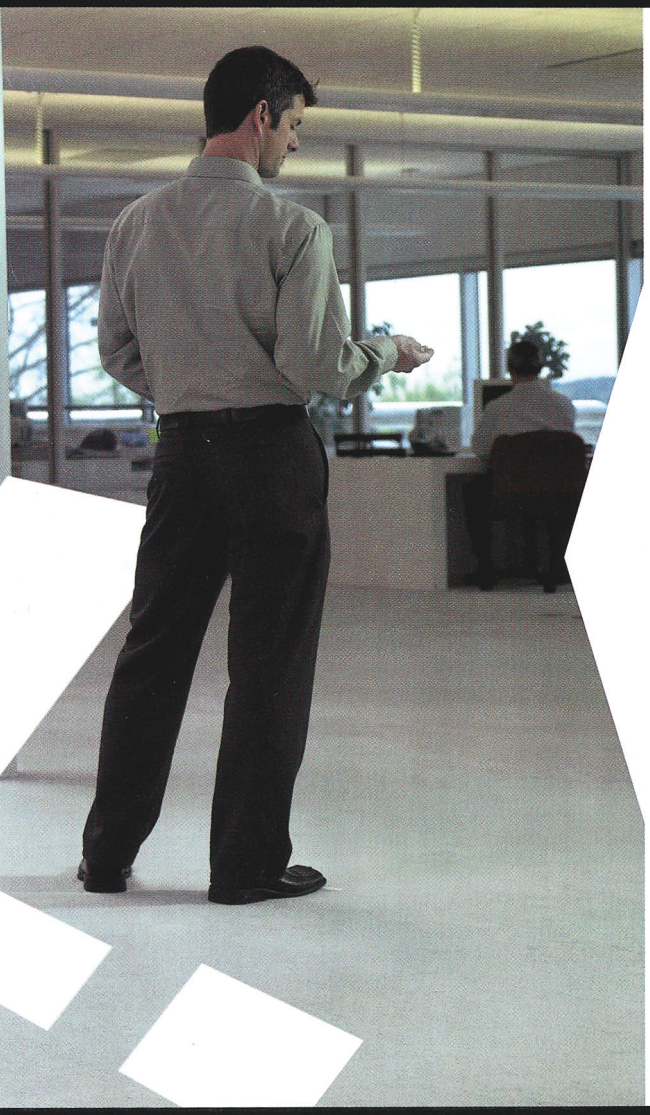

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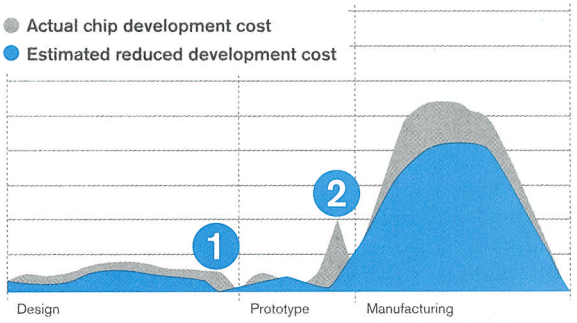
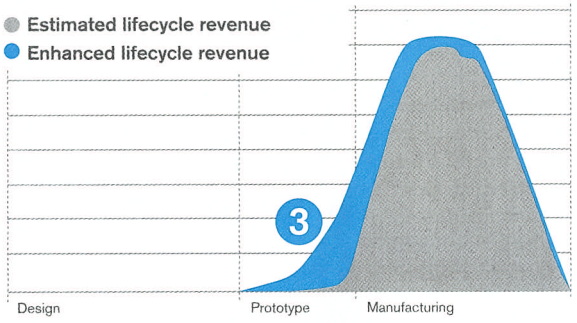


Chip Lifecycle Revenue



Source: Semiconductor Lifecycle Cost Study, 2005

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To learn more about predictable success and to get your copy of the Semiconductor Lifecycle Cost Study, visit synopsys.com/success.

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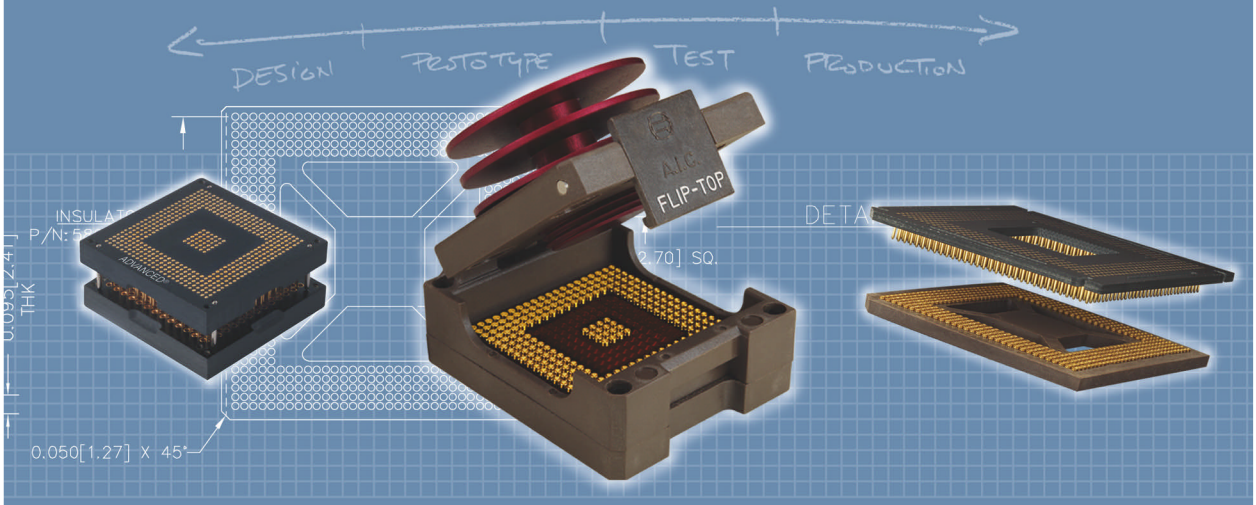

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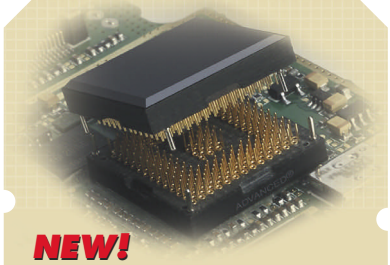

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INNOVATIONS & INNOVATORS

Immersion-lithography road map hits dead end

As the promise of EUV (extreme-ultraviolet) lithography fades, the old war-horse, 193 nm, is again rising up to fill the gap. By immersing the wafer and the front element of the lens in water, stepper vendors have been able to edge up the numerical aperture and the depth of field of their optical columns just enough to make 65-nm fabrication ready for production and probably enough to make the 45-nm node feasible. However, the next step, to 32 nm, could be costly and may be a step too far.

The lithography heavyweights, ASML and Nikon, were at Semicon West in force in July with their advanced 193-nm immersion systems. Canon, which appears to have lost ground to the leaders in the race toward 45 nm, was discussing a development platform rather than a production stepper. Everyone voiced a certain amount of confidence that the systems, which pump highly purified water through a puddle that contacts both the objective lens and the wafer, will also form the basis of 45-nm production.

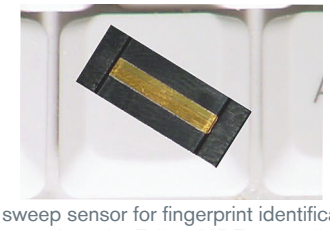
Immersion lithography helps because the light leaves the objective lens into a fluid—water—with a higher refractive index than air. To increase the depth of field, numerical aperture, or both for 32-nm work, developers must find a fluid with an even higher refractive index. The refractive index of pure water is simply too low for 32-nm work. According to Ludo Deferm, vice president of business development at European research consortium IMEC (Interuniversity Microelectronics Center), all of the fluids that vendors have so far tried either are too viscous to remain uniform as the wafer passes under the objective at high speed or are chemically reactive with the objective-lens coatings, the photoresist, or both. So far, no one has been able to solve the materials problem, leaving some unpleasant alternatives. Critical layers will depend on double-exposure techniques using two masks, according to Deferm. You expose each mask using an off-axis lighting pattern to produce the desired image on the resist. This technique appears to be able to produce the feature size that 32 nm requires, but it demands additional masks and additional stepper time, both of which are hits to cost.**—by Ron Wilson**

▷**ASML**, www.asml.com.
▷**Nikon**, www.nikon.com.
▷**Canon**, www.canon.com.
▷**IMEC**, www.imec.be.

Biometric sensor and preboot software lock down laptops

A handful of companies has for a number of years been pitching biometric sensors as the best protection for portable PCs and other electronics, and the technology is catching on with some enterprise-IT departments. But a technology such as a fingerprint sensor needs software support to supplant or complement a password in protecting notebook-PC data. So, Fujitsu Microelectronics turned to software partners Phoenix Technologies and Cogent Systems for support in launching its latest sweep sensor, the MBF 320.

The trio is offering a fingerprint sensor that is active before the operating system boots in a package that eases OEM-implementation challenges. Although you must configure the USB 2.0-based sensor at the operating-system level, it operates at the BIOS level after configuration. Phoenix supports the sensor in its TrustedCore firmware, and more than 50% of the company's BIOS customers now ship the TrustedCore software. Meanwhile, Cogent provides the fingerprint-matching engine that the TrustedCore BIOS hosts. The three components offer OEMs a turnkey approach to adding biometric security.



A sweep sensor for fingerprint identification, such as the Fujitsu MBF 320, relies on a narrow array of sense elements, allowing the sensor to occupy minimal space in products such as notebook computers and even handheld devices.

The Fujitsu sensor hosts a 500-dpi, 8×256-pixel sensing array and 8-bit grayscale depth. The sensor includes an automatic-finger-detection feature that wakes the sensor. In standby mode, the sensor sips less than 200 µA of current. When active, the sensor draws less than 12 mA of current. Samples are now available for $5 (1000). The software bundle also supports Fujitsu's older, 2-D MBF 200 single-touch sensor.**—by Maury Wright**

▷**Fujitsu Microelectronics**, http://us.fujitsu.com/micro/biometricsensors.
▷**Phoenix Technologies**, www.phoenix.com.
▷**Cogent Systems**, www.cogentsystems.com.

Speedy Spice-accurate simulator targets analog, RF

Most analog and RF engineers rely on Spice simulators for accurate circuit analysis, but Spice simulation is painfully slow. Over the years, EDA vendors have attempted to speed Spice simulation for engineers by introducing fast-Spice simulators. Although the tools speed simulation, they compromise accuracy. Officials at Berkeley Design Automation believe they have solved this problem with two tools that the company claims are Spice-accurate and five to 10 times faster than competing tools.

According to EDA veteran Paul Estrada, Berkeley's chief technology officer, the company merged its patented, stochastic, nonlinear simulation engine from its PLL-Analyzer tool with a range of tools. These tools are a fast, sparse-matrix solver; a global-convergence solver; adaptive time-stepping technology; latency-exploitation algorithms; a fast, stiff-DAE (differential-algebraic-equation) solver; a unified time/frequency engine; and a device-sensitivity analyzer. Together, these tools create the Analog FastSpice time-delay, or transient-analysis, simulator and the RF FastSpice periodic-convergence-analysis add-on for Analog FastSpice.

Tom Ferry, the company's vice president of marketing, says the tools target simulation of large, critical blocks, giving analog and RF engineers a reliable and accurate fast-Spice-class tool. He notes that most fast-Spice tools use a divide-and-conquer approach: They piece a design into mini blocks, and users then tune the blocks' performance before they simulate their circuits. In some cases, tuning blocks can take more time than running a pure-Spice simulation. The Berkeley tools, in contrast, do not break down circuits into mini blocks and require no tuning, says Ferry. Instead, users input their Spice netlist into the tool and then simply run the simulation.

"The result of this technology is an order of magnitude improvement in verification bandwidth," says Ferry. "If you are designing an RF CMOS or a 65-nm SOC [system on chip] with 32 SERDES [serializer/deserializer] ports on it, having this much more bandwidth is amazing." Beta customers have run the Analog FastSpice tool on several designs. A SERDES-circuit design comprising 4200 devices in a 0.13-micron implementation took 5.4 days to run in pure Spice but only 7.2 hours with Berkeley's tool, Estrada claims. The company ran benchmark tests of its tool versus pure Spice on several 802.11 circuits targeting 0.18-micron technology. A 107,264-device IC took 1.2 hours to run in pure Spice and nine minutes to run in Analog FastSpice. At the other end of the spectrum, a complex circuit with 25,522 devices took 6.25 days to run in pure Spice but only 15 hours with Berkeley's tool, Estrada claims.

In benchmarking the RF FastSpice against the most popular commercial simulator, the commercial simulator couldn't finish most designs, the pure-Spice tool was unable to finish four of the seven benchmarks, but RF FastSpice completed them all. The simulator completed a digital-TV circuit with 8590 devices in 28 minutes and another TV circuit with 6548 devices in 10 minutes. The pure-Spice tool finished one wireless circuit in 45 minutes, a second wireless in 100 minutes, and a networking circuit in 40 minutes, compared with 4.5 minutes, 100 seconds, and four minutes, respectively, for the RF FastSpice.

The RF version of FastSpice supports complex blocks, such as a voltage-controlled oscillator, a crystal oscillator, a low-noise amplifier with a mixer circuit, and a power-amplifier circuit. The company tailored the tools to plug into the Cadence (www.cadence.com) Virtuoso ADE (analog-design-environment) flow. The tools are compatible with HSpice and Spectre netlists, and they run with traditional models, such as BSIM (Berkeley short-channel IGFET model) 3 and 4, Verilog-A, and s-parameter. Analog FastSpice costs $95,000 for a one-year subscription, and RF FastSpice costs $40,000 for a one-year subscription.

—by Michael Santarini

▷**Berkeley Design Automation**, www.berkeley-da.com.

FROM THE VAULT

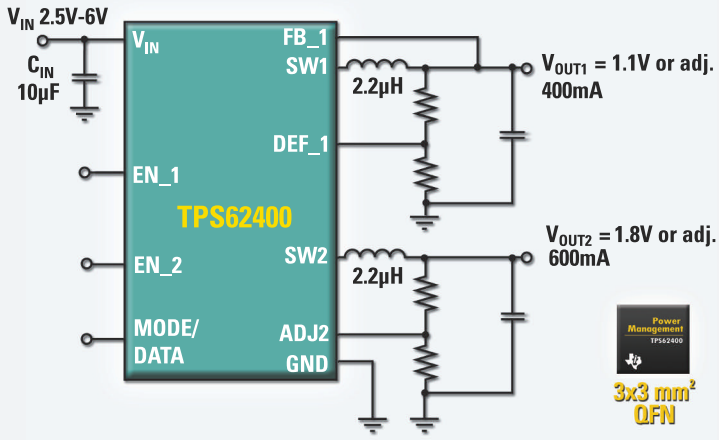
Are engineers handicapped in reaching the highest levels of corporate management? According to a lengthy study conducted by AT&T, they might be. The results of that study, ongoing since the 1950s and reported by industrial psychologist Ann Howard in the proceedings of the 1983 IEEE Careers Conference, suggest that engineers are unlikely to have the interpersonal, verbal, and administrative skills most companies consider important managerial attributes. Further, the study indicates that graduates of social-science and humanities programs typically surpass engineers in these key management skills and are much more likely to reach high-level positions.

Gary Legg, Editor, *EDN*, April 19, 1984, pg 55

DILBERT *By Scott Adams*

POWER MANAGEMENT

Dual Buck Converter with 1-Wire Interface



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TPS62350	Buck	800	2.7 to 6.0	0.75 to 1.537	3000	12-pin WCSP	$2.15
TPS717xx	LDO	150	2.5 to 6.5	0.9 to 6.2	—	5-pin SC70	$0.45
TPS799xx	LDO	200	2.7 to 6.5	1.2 to 6.5	—	5-pin WCSP	$0.35

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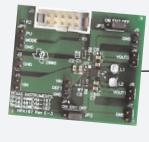

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Free tool tracks verification plans

Formal-verification-tool start-up Jasper Design Automation is offering a free tool to help IC-verification teams generate and track verification plans. Craig Cochran, vice president of marketing at Jasper, says that the company offers "lite-" and deep-formal tools. Lite-formal tools, such as JasperGold Express, typically prove formal assertions, whereas deep-formal tools, such as JasperGold, run a systematic formal test plan describing the most critical features in a design that require formal verification. The tools then systematically verify the features.

Most verification teams use a mixture of simulation, formal, code-coverage, and other techniques. "You still use your simulator, do constrained random verification, and use coverage-driven verification to see blanket coverage across a design," says Cochran. "But the blanket coverage is still uncertain because you can't achieve full coverage with just a simulator. All features of your chip are not created equal. Some functions can be crucial to your chip because of complexity, a new feature, or even a late spec change."

Verification teams must prioritize these functions and figure out what verification techniques best suit each function. So, verification teams typically devise a verification plan. "Customers have been writing these test plans for some time, but they usually write them with a word-processing program," says Cochran. "There really was a need for a tool that would help people easily create and generate a test plan. People could get a lot of use out of this product—not just for formal verification, but also for simulation."

Jasper plans to give away copies of its GamePlan Verification Planner beginning in the next few weeks to anyone who is interested in downloading it. The product helps users capture the main features, expected functions, verification approaches, test priorities, technologies, and test status of their design. The tool generates a verification-test matrix to provide the overall verification status and generates a verification-test plan in hyperlinked HTML (Hypertext Markup Language) format. Verification teams can share the test matrix and HTML-verification-test plan over their network to share information on their progress.

Jasper created GamePlan's test-plan structure in customizable XML (Extensible Markup Language). The tool isn't Jasper-specific and doesn't require users to have a copy of JasperGold Verification System or JasperGold Express to run it. You can check out the status and when the download will be available at www.jasper-da.com/gameplan.

—by Michael Santarini

▷**Jasper Design Automation**, www.jasper-da.com.

09.01.06

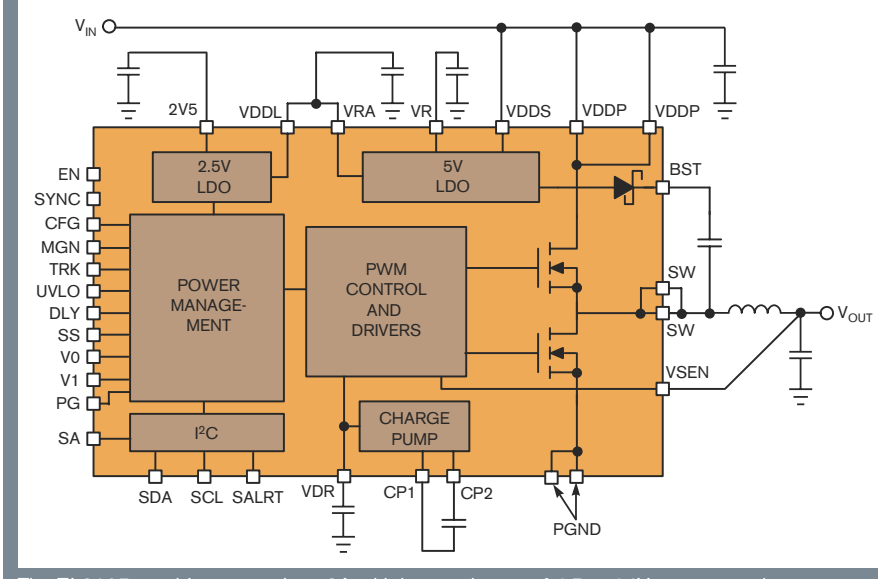
Power-conversion and -management IC squeezes into embedded-system space

Zilker Labs' new ZL2105 digital-power-conversion and -management IC targets the needs of the embedded-system market. The device provides as much as 3A at 0.6 to 5.5V. The chip combines power-management and -conversion functions, as well as the switching FETs, into its 6×6-mm package.

Unlike several other digital-conversion ICs, which use PID controllers for their PWM schemes, the ZL2105 uses a state machine. "The architecture is deterministic: You can't change it from being a buck step-down converter, because the loop is a hard-wired state machine—not a DSP or a microcontroller," says Jim Templeton, Zilker's founder and vice president of marketing. "That's part of the ease of use of the chip, because it makes it higher efficiency by virtue of dissipating less power," he adds.

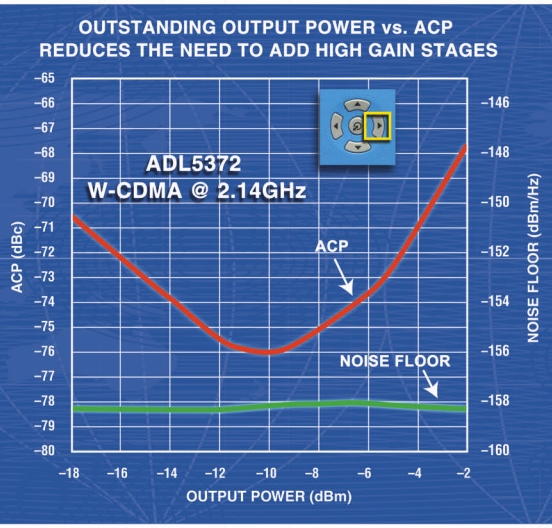
The chip requires no programming: You set characteristics such as output voltages, overcurrent-protection settings, delay times, and more by strapping pins, selecting resistors, or using any of the PMBus commands that the chip supports. The device costs $2.80 (100).—by Margery Conner

▶**Zilker Labs**, www.zilkerlabs.com.



The ZL2105 provides as much as 3A with input voltages of 4.5 to 14V at output voltages ranging from 0.6 to 5.5V. It includes integrated switching FETs and a boost diode and requires no programming.

RF modulators with the highest linearity and output power.
In RF designs, analog is everywhere.



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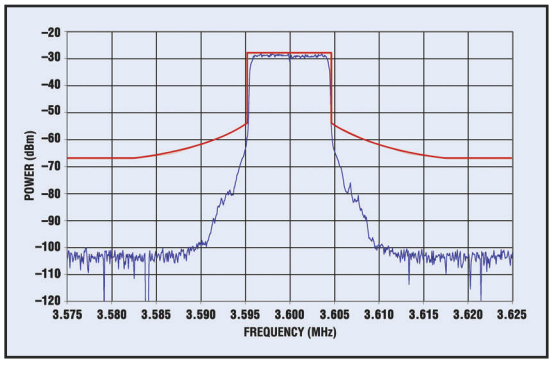
ADL537x family of pin-compatible RF modulators

ADL5370 ADL5371 ADL5372 ADL5373 ADL5374

Part Number	Center Frequency (MHz)	Frequency Range (MHz)	OIP3 (dBm)	P1dB (dBm)
ADL5370	450	250 to 1300	23	10.5
ADL5371	900	700 to 1300	26	13.5
ADL5372	2140	1600 to 2400	26	12
ADL5373	2500	2300 to 3000	25	13
ADL5374	3500	2800 to 4000	21.5	11



ADL5374 WiMAX spectrum at 3.6 GHz, carrier power = –10 dBm.

Best dynamic range for direct transmit designs from 250 MHz to 4 GHz

Our new RF modulator family offers the highest output power and widest dynamic range, across all radio standards and frequencies. These pin-compatible devices generate highly linear modulated RF signals that improve transmission quality and eliminate the need for intermediate frequency stages. The ADL537x modulators are optimized for specific bands of operation and offer:

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Modular instrumentation: LXI challenges PXI

The PXI (PCI Extensions for Instrumentation) open, modular standard emerged almost a decade ago. The industry widely considers PXI the successor to the physically larger VXI (VME Extensions for Instrumentation). Overall, PXI is a success; its recent growth far exceeds that of test and measurement as a whole. Still, not everybody is satisfied with PXI. Among those who feel that the industry needs a different standard is Agilent Technologies (www.agilent.com), the world's largest test-and-measurement-product supplier. Agilent and several other manufacturers have formed the LXI (LAN Extensions for Instrumentation) Consortium (www.lxistandard.org) and have begun to introduce products that conform to a standard that differs markedly from PXI. Recently, *EDN* asked representatives of LXI and the PXI Systems Alliance (www.pxisa.org) to explain why they believe that their camp offers the best modular-instrumentation approach. Read abbreviated versions of the comments here; then go to www.edn.com/060901p1 for the full story.

PXI No single bus is ideal for every application. USB is excellent for easy desktop connectivity, LAN/Ethernet suits use in distributed systems, and PCI and PCI Express provide high performance for automatic test equipment. For applications demanding a modular approach, users should expect reduced cost and size through a shared chassis, backplane, and processor; greater throughput through a high-speed connection to the host processor; and greater flexibility and longevity through user-defined software.

PXI, based on PCI and next-generation PCI Express, is the fastest growing test-and-measurement standard since IEEE 488. PXI best meets modular-instrumentation demands, with more than 70 vendors in the PXI Systems Alliance, more than 1200 products, and a projected 25%-annual-growth rate through 2011, according to Frost and Sullivan (www.frost.com). All instruments in a PXI system share the same power supply, chassis, and controller. With PXI, the controller can be a high-performance slot-zero embedded controller, a desktop or laptop PC, or a server-class machine. When you require faster processing, you can easily upgrade a PXI system's controller. To reuse existing equipment, you can use PXI to control USB, IEEE 488, LAN/LXI, serial, and VXI instruments.

Modular instruments require a high-bandwidth, low-latency bus to connect instrument modules to the shared processor for performing user-defined measurements. PXI meets these needs with bandwidth as high as 2 Gbytes/sec for each slot. In a modular RF acquisition system, PXI can stream two channels of 100M-sample/sec, 16-bit intermediate-frequency data directly to a processor for computation. Neither LAN nor USB can meet these requirements, so these instruments always include an embedded, vendor-defined processor. Only high-bandwidth standards, such as PXI, provide a truly software-defined approach for modular instrumentation.

—by Darcy Dement, senior product manager, National Instruments

LXI LXI is the successor to IEEE 488 that simplifies system integration by leveraging Ethernet's position as the most popular communication protocol. LXI offers an easy transition from IEEE 488 because there is no software to change, and the specs remain the same. Further, designers can use non-LXI equipment in hybrid systems by adding bridges and adapters.

But LXI goes further by offering capabilities never before available. LXI simplifies setup, control, troubleshooting and test-asset management. It can enable remote operation or sharing in which engineers at different sites can access and control an instrument. The IEEE 1588 PTP (Precision-Time Protocol) adds the dimension of time to the system designer's arsenal. Finally, the LXI infrastructure is simple: LAN cards are standard on all computers, cables cost pennies per meter, and inexpensive routers and switches are readily available.

LXI is also highly scalable, allowing designers to buy only what they need when they need it. Modular architecture allows engineers to mix and match measurement resources and add channels, I/O lines, switches, signal resources, and modules without card-cage-slot constraints. LXI boosts efficiency by enabling software written for R&D instruments to run on finished modules, ensuring traceability through the product life cycle. Smart modules distribute intelligence to the network and improve efficiency by running application-and-analysis software locally. The result is less programming and less traffic between instrument and controller, leaving more bandwidth for data-analysis tasks.

LXI boosts speed by offering 125 times the I/O throughput of IEEE 488. Time stamps reduce troubleshooting times by months, and remote operation allows engineers at different sites to remotely troubleshoot problems. LXI's high-speed LVDS (low-voltage-differential-signaling) trigger bus operates in star or daisy-chain configurations to deliver ultrahigh-speed, low-latency, low-jitter signals to applications requiring direct links between two devices.

—by Bob Rennard, president, LXI Consortium

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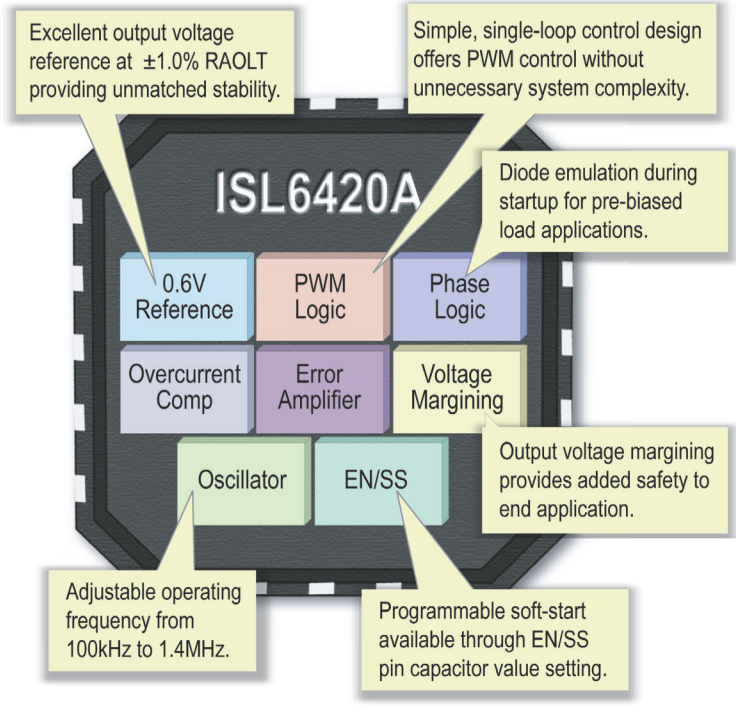
Intersil knows that different applications have different design needs. That's why we've created the ISL6420A wide V_{IN} Step Down Controller. In addition to the flexibility to support multiple input voltages, this device combines control, output adjustment, monitoring and protection into a single package.

The ability to address a wide input voltage range of 4.5V to 28V gives the ISL6420A unmatched flexibility for use in most general purpose applications. It also has resistor-selectable switching frequency from 100kHz to 1.4MHz. Add all this up and Intersil has made choosing the right switching regulator for your design...well, like a day at the beach.



Key Features:

- Operates from 4.5V to 28V input
- Excellent output voltage regulation with 0.6V internal reference with ±1.0% RAOLT
- Resistor-selectable switching frequency from 100kHz to 1.4MHz
- Voltage Margining and External Reference Tracking
- Output can sink or source current
- Lossless, programmable overcurrent protection using upper MOSFET's rDS(on)
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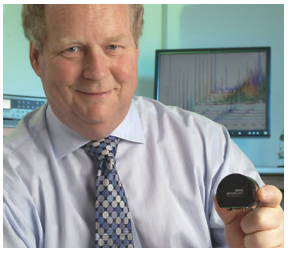
Vibration powers wireless sensor

The idea of wireless sensors that report measurements over communications protocols, such as 802.15.4, including ZigBee and other similar standards, is gaining ground. A key part of the concept is that such sensors—with their low power demand and duty cycle—should derive their power from batteries or should extract their power requirements from energy they "harvest," or "scavenge," from the environment. Start-up company Perpetuum has designed its PMG7 generator to glean sufficient energy from the vibration of rotating equipment—pumps, fans, and other mechanical equipment—that ac-induction motors drive to power a sensor and wireless-transceiver node.

Perpetuum's generator is electromechanical rather than piezoelectric, a principle that some researchers have used to scavenge vibration energy. Its fundamental structure is a sprung beam that carries a pair of permanent magnets. Vibration sets the magnets in motion, and a coil comprising many turns of fine wire lies between the magnets. Circuitry in the generator rectifies the ac and charges a capacitor or supercapacitor, which in turn powers the sensor node. The design can gather useful amounts of energy because the sprung beam is a resonant structure, tuned to the 50- or 60-Hz vibrations that all ac motors produce. The essence of the Perpetuum product is the design of the resonant beam, which has a wide mechanical bandwidth; a range of vibration frequencies set it in motion, and users need not tune each generator to a specific motor. The generator offers a mechanical-tuning feature, but Perpetuum's Chief Executive Officer, Roy Freeland, asserts that the PMG7 works immediately when you attach it to almost any ac motor driving mechanical equipment. Freeland believes that such a power source is essential for the deployment of 802.15.4 networks: "When you present the wireless-sensor idea to, for example, process engineers, they are enthusiastic until you mention the word 'battery,'" he says. "We know of an oil company that will not accept any form of battery-powered equipment on its sites."



The PMG7 generator gleans sufficient energy from the vibration of rotating equipment—pumps, fans, and other mechanical equipment—that ac-induction motors drive to power a sensor and wireless-transceiver node.

The PMG7 generator outputs at much as 5 mW at 3.3V from a vibration level of 100 mg. This power is sufficient to drive a wireless node to periodically report sensor data, such as temperature, pressure, or the spectrum of the same vibrations that power the generator. US manufacturer RLW Inc (www.rlwinc.com) has employed this principle to build its accelerometer-based condition-monitoring sensor node. It transmits raw-accelerometer spectrum for remote analysis, but Perpetuum says enough energy is available to perform an FFT within the sensor and to report processed data. Users can bolt a sensor node to the motor, pump, or fan housing, or they can simply and temporarily attach a magnetic clamp for true "instant-sensor-network" operation.

Perpetuum's target price for high-volume production is less than €100. Its price at introduction is higher, but Freeland says: "The product is already competitive with a battery-powered alternative when you take into account the lifetime cost of using batteries and include the cost of intervention by service personnel to replace them."

—by Graham Prophet, *EDN Europe*

▷**Perpetuum Ltd**, www.perpetuum.com.

09.01.06

Spectrum analyzer adds phase-noise-measurement set

Rohde & Schwarz's new FSUP signal-source spectrum analyzer and phase-noise tester tests and characterizes RF-signal sources. It operates at 8, 26.5, or 50 GHz, depending on options. A typical task in developing a communications system is measuring an oscillator's phase noise, harmonics, settling, or power in the adjacent channels and testing transmitter and receiver modules; the device performs all these functions in one unit. The instrument compares the signal under test with an internal or external reference; an option adds a second receiving path to the instrument, allowing users to assess the correlation between two signals. The instrument provides phase noise with an internal reference source of −136 dBc at 1 Hz at a 64-MHz input frequency and 10-kHz frequency offset and −165 dBc at 1 Hz at 10-MHz frequency offset.

The device allows users to mark and list all interference lines or to suppress interference lines. It also displays integral parameters, such as residual frequency- or phase-modulated jitter or rms jitter. The phase-noise tester can record the level or the frequency of the signal source as a function of time, allowing you to track settling and switching of transitions in high-frequency signals, monitoring their behavior in the time domain. The instrument includes high-stability dc sources to assist in characterizing the behavior of voltage-controlled oscillators.

Rohde & Schwarz's new spectrum analyzer allows users to mark and list all interference lines or to suppress interference lines. It also displays integral parameters, such as residual frequency- or phase-modulated jitter or rms jitter.

Combining a spectrum analyzer and a phase-noise tester allows users to reduce the cost of making a set of measurements that are typical of those that today's RF- and radar-signal waveforms require.

—by Graham Prophet, *EDN Europe*

▶**Rohde & Schwarz**, www.rohde-schwarz.com.

Intersil Voltage Supervisors

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Need More Voltage Supervisor Options?

Whether you need adjustable or fixed voltage monitoring, dual or single voltage supervision, or even enhanced functionality such as Power On Reset or Watchdog Timer, Intersil's ISL8801X Voltage Supervisors deliver superior performance with 1.5% trip point accuracy.

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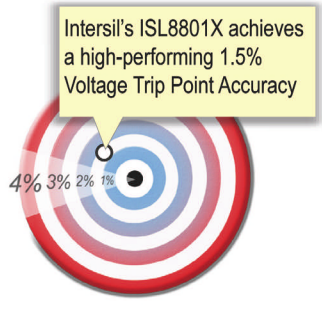
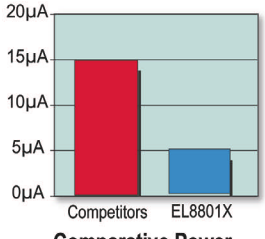
ISL8801X Family's Available Features and Functions	ISL88011	ISL88012	ISL88013	ISL88014	ISL88015
Active-Low Rest ($\overline{RST}$)	●	●	●	●	●
Active-High Rest (RST)	●	●	●		
Watchdog Timer (WDI)			●		●
Dual Voltage Supervision		●			
Adjustable POR Timeout (C_{POR})	●			●	
Manual Reset Input ($\overline{MR}$)	●	●	●	●	●
Fixed Trip Point Voltage	●	●	●		
Adjustable Trip Point Voltage		●		●	●



Voltage Trip Point Accuracy Over Temperature



Comparative Power Consumption

- Small SOT-23 Pb-free package
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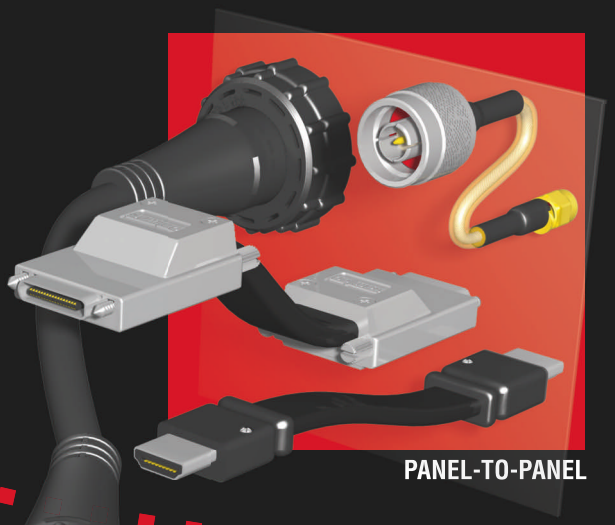
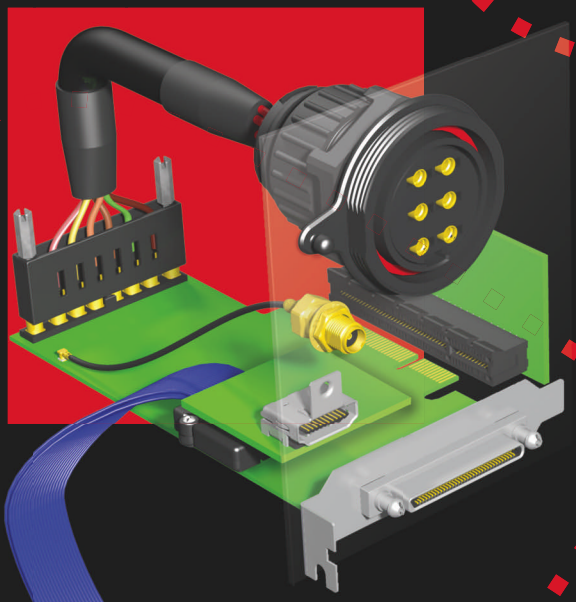


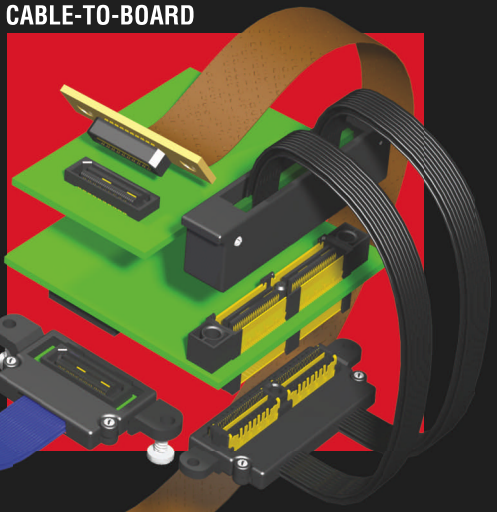
PANEL-TO-PANEL

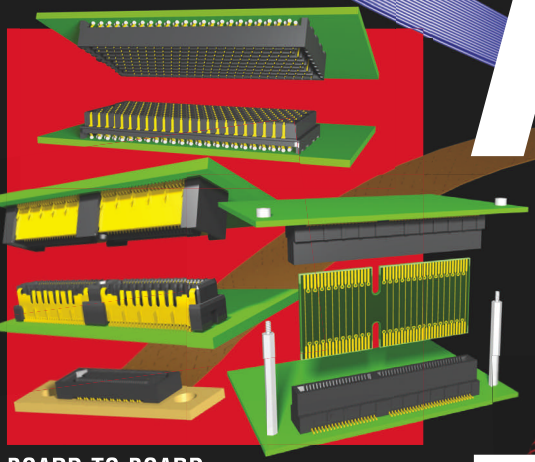
PANEL-TO-BOARD



FROM THE OUTSIDE IN

CABLE-TO-BOARD





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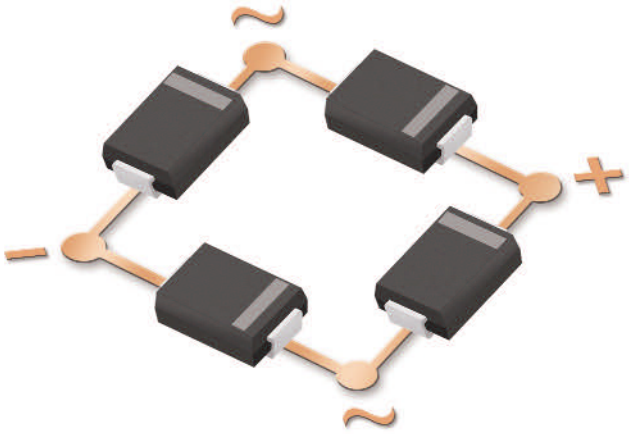

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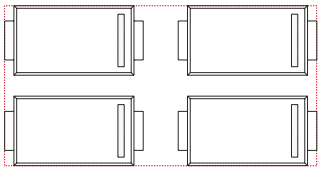
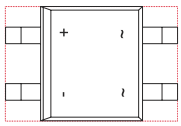


4 SMA packages



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BY BONNIE BAKER

Using Spice to ease your life

A computer-based simulation of your analog and digital circuit is important. Such a simulation is important because using your preferred computer Spice program for analog simulation or IBIS (I/O Buffer Information Specification) program for digital simulation can reduce initial errors and development time. If you correctly use your simulator, you can identify circuit errors and nuances before you go to your breadboard. The first step to correctly using these tools is to determine the expected performance of your circuit before you start simulations. Then, after you run a simulation of your circuit, you verify your design before you spend time soldering the circuit. These tools also help you to troubleshoot your bench circuit. Using simulations is a great way to try out ideas by creating what-if scenarios.

You can view the results from these software tools on a PC with user-friendly graphical-user-interface suites. These tools fundamentally provide dc operating points, small-signal gain, time-domain behavior, and dc sweeps. At a more sophisticated level, they help you analyze harmonic distortion, noise power, and gain sensitivity and perform pole-zero searches. This list is incomplete, but generally, Spice and IBIS software have many of these fundamental features. By finessing the Monte Carlo and worst-case-analysis tools in Spice, you can predict the yields of your final product. At the onset of a project, using a breadboard circuit may be expensive and time-consuming. A simulation may speed up your application-circuit time to market.

But beware. You can effectively evaluate analog and digital products if your models or macromodels are accurate enough for your application. The key words here are "accurate enough." These models should mimic the actual performance of the component without carrying the burden of too many circuit details. Too many details can lead to convergence problems and extremely long simulation. Too few details can hide some of the intricacies of your circuit's performance. Worse yet, your simulation, whether you use a complete circuit model or just the macromodels, may misrepresent what your circuit will do. Remember that a Spice or an IBIS simulation is simply a pile of mathematical equations that, with any luck, represents what your circuit will do. In essence, a simulation produces imaginary results.

You can effectively evaluate analog and digital products if your models or macromodels are accurate enough for your application.

The nay sayers in the industry will tell you that your computer-based-simulation tools do not work and that using them is a waste of time. These people are a bit misguided and have a limited view of what these tools can do. Sure, if you misapply a Spice tool, it can lead you astray. These simulation tools do not replace good engineering judgment. But, like any other tools, they are only as good as their users. Before you run a simulation, it is critical to have a good idea of how the final outcome will look. Any insight that you gain from your simulations is a bonus. Better yet, Spice simulations point out problems that you would never anticipate. In most cases, these simulation tools use double-precision calculations. Such calculations ease the detection of low-level problems that are impossible to find on the bench.

The questions are: Does my model accurately mimic the device over temperature? Does the simulation produce distortion results that are representative of the device? Do I receive a good portrayal of the device's ac response? Do I expect the model to simulate these parameters and to what degree of accuracy? What information do my models provide? Did I accurately include the parasitic characteristics of my board and components?

The only way to answer these questions is to have a feel for what your circuit will do in real life before you start your simulations. Then, ask challenging questions about your simulation results. There is no replacement for good engineering judgment. EDN

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Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

A function generator set for action

The Agilent 33220A packs in bench and test-system features

Agilent 33220A 20 MHz function/arbitrary waveform generator

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- *Open connectivity via USB, LAN, and GPIB*

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The Agilent 33220A function generator packs outstanding performance into a very compact design.

Able to fit into your rack or on your bench, the 33220A is loaded with multiple signal powers—from stable, accurate output of low-distortion sine waves to variable edge-time pulses and custom arbitrary waveforms.

Front panel operation provides the ease of use you'd design yourself—because Agilent created the 33220A in consultation with customers like you. You'll find access to all major functions and adjustments at your fingertips. Agilent Open capabilities mean system readiness, compatibility with popular software environments, plus built-in USB, LAN, and GPIB ports.

The Agilent 33220A is powerful and affordable enough for uses from R&D to manufacturing. Its software compatibility with the widely used 33120A and 33250A function generators ensures easy integration into new or existing systems. To enhance your function generator power now, get tips at www.agilent.com/find/8-hints.

Agilent Technologies

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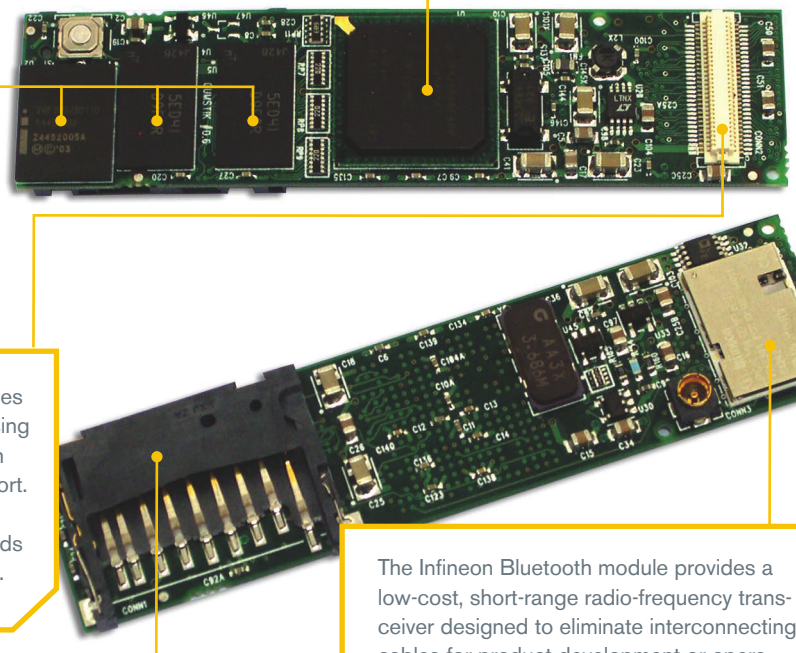
Tiny computer holds embedded treasure

The Waysmall series from Gumstix offers designers a line of Linux-based computer systems that easily fit into the palm of your hand. Housed in an 83×36×15-mm plastic case, these miniature systems provide XScale processing power along with an MMC (MultiMedia Card) slot, two serial ports, one USB client port, a power interface, and general-purpose I/O pins. Introduced in 2004 and selling for less than $200, Waysmall computers are popular with the open-source community for mobile- and handheld-system applications. But the real treasure for embedded-system designers is hidden inside: a complete single-board computer that is literally the size of a stick of gum.

A 200- or 400-MHz Intel XScale processor powers the Gumstix single-board computer, which measures 80×20×6.3 mm. Targeting low-power, open-source applications, all Gumstix configurations run the 2.6 Linux kernel and user-space tool kit based on the embedded C library and the Busybox utilities. The software offers a complete Linux operating-system environment plus a range of open-source applications that can run on the single-board computer.

The single-board computer includes 64 Mbytes of SDRAM and 4 or 16 Mbytes of Strataflash. Flash memory comes preloaded with Bluetooth utilities, HTTP-server and -client routines, audio players, and uClibc, a small-footprint C library for embedded Linux systems. You can also add a wide range of system, communications, scripting, library, and development tools to the Gumstix platform using the supplied build-root configuration tools.



The Gumstix single-board computer attaches to the Waysmall computer motherboard using a 60-pin Hirose connector to interface with the power source, serial ports, and USB port. Although somewhat fragile, this connector enables a variety of Gumstix expansion cards or application-specific custom baseboards.

The card slot adds as much as 512 Mbytes of flash memory for program or data storage. For size-constrained applications, Gumstix offers a reduced-size flash-memory card that fits inside the MMC socket footprint. Gumstix designers were forced to use MultiMedia instead of SD (Secure Digital) cards because open-source drivers would reveal the proprietary encryption scheme. Optional single-board-computer configurations replace the MMC slot with a second I/O connector to enhance expansion features.

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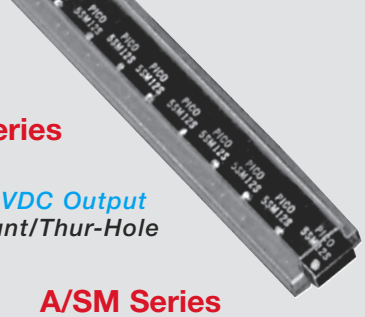

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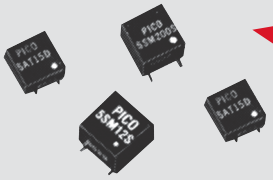

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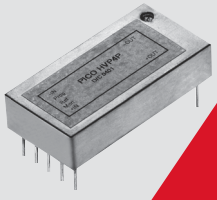

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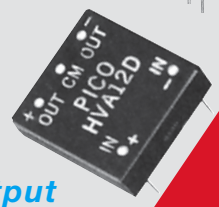

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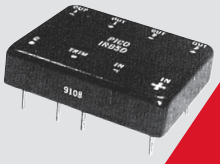

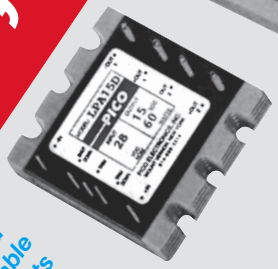

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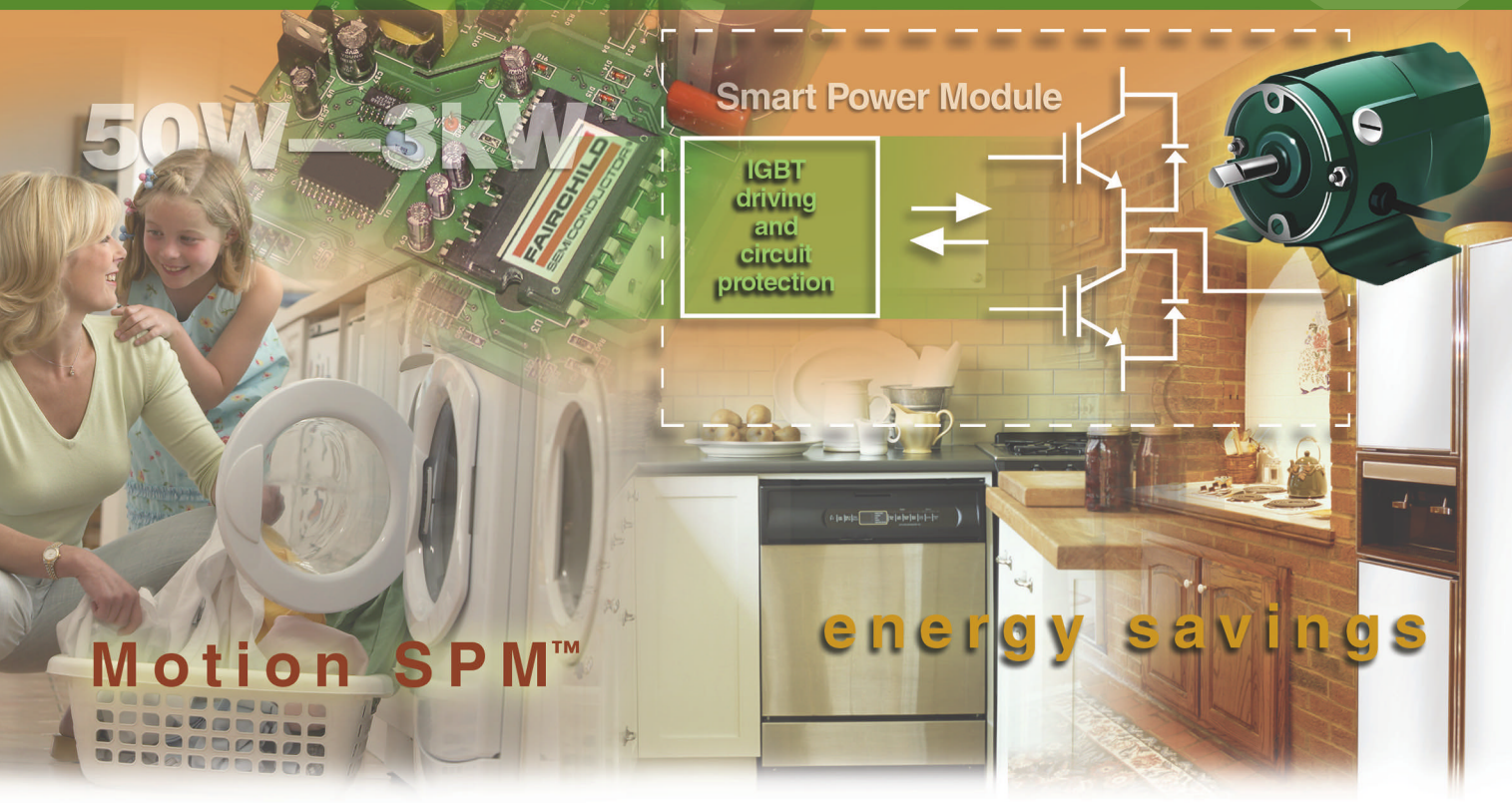

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Figure 1 The Belkin CableFree USB hub allows USB 2.0 devices to plug into a hub that connects wirelessly to a PC through a plug-in adapter.

BY RICHARD A QUINNELL • CONTRIBUTING TECHNICAL EDITOR

CLASH OF THE WIRELESS-USB STANDARDS

WIRELESS USB IS POISED TO ENTER THE MARKET. UNDERSTANDING THE DIFFERENCES BETWEEN THE TWO LEADING APPROACHES WILL HELP DEVELOPERS CHOOSE THE RIGHT ONE FOR THEIR APPLICATION.

Becoming wireless is a natural step in the evolution of the popular USB (Universal Serial Bus), whose developers aimed at simplifying the cabling of PC systems. Now, two approaches to unwiring the USB have arisen, leaving developers with the difficult choice of which to pursue. Making that choice requires understanding the differences between these two approaches and the trade-offs those differences represent.

The clash of the wireless-USB standards did not begin with the computer community; it came from the wireless industry. Wireless-system developers were looking for a means of establishing short-range, high-speed data communications that did not conflict with other users of the increasingly crowded radio spectrum. The answer that arose was the UWB (ultrawideband) radio, which works by spreading its radiated energy over many gigahertz, so that it is too weak to interfere with conventional users of the same frequencies.

Two UWB schemes appeared: DS (direct sequence) and OFDM (orthogonal frequency division multiplexing). Supporters of each approach—the UWB Forum for DS-UWB and the WiMedia Alliance for OFDM-UWB—worked to get the IEEE to adopt their technologies as IEEE standards, but the standards process stalled. That standards conflict has now spawned a market battle for the "killer application" of UWB: a wireless version of the USB. The two main contenders are the CableFree USB, which Freescale Semiconductor and its partners promote, and the Certified Wireless USB, which the

AT A GLANCE

- Two approaches to wireless USB are poised to hit the market.
- Protocol differences are more significant than radio differences.
- CableFree USB uses USB 2.0 for low cost and ease of implementation.
- Certified Wireless USB uses a new protocol for wireless links.
- Key protocol differences involve the handling of association, security, and signal-integrity issues.

WiMedia Alliance and the USB-IF (USB Implementers Forum) promote.

Perhaps surprisingly, the most significant differences between these clashing wireless standards occur in the communications protocol, not the radio link. There are radio differences, but the operations of the unwired-USB approaches are relatively indifferent to such physical-layer details (see **sidebar** "A tale of two radios"). The real differentiation comes in how each approach handles the problem of using a radio in the first place.

Replacing a cable with a wireless link is more difficult than it looks. The replacement link must do more than simply pass along a copy of the bits coming in at each end. It must replace some attributes of a wired connection that are absent from wireless ones, including reliable signal integrity, inherent association, and physical security.

CABLE-REPLACEMENT ISSUES

Signal integrity becomes an issue for wireless-cable replacement, because wired-communications protocols usually expect a highly reliable data stream. Without special provisions for handling the kinds of delayed or dropped data that can occur with a wireless link, wired protocols can quickly fail. The USB protocol has only a few features to deal with signal issues. One is a CRC (cyclic-redundancy check) to detect noise-corrupted data packets. Another is a turnaround timer to prevent the bus from waiting forever for a failed peripheral to respond to the host.

The CRC poses no special problems for a wireless link, but the turnaround timer can. The delays inherent in converting the bit stream to a modulated radio signal, and the corresponding demodulation, may be more than the turnaround timer can tolerate. Switching delays may also exist in the wireless channel when the system must use the same antenna for both transmitting and receiving, aggravating the problem.

The issues surrounding association are artifacts of the wireless link's broadcast nature. "Association" means establishing a well-defined logical connection from one device to another. Defining a connection is inherent in a cable hookup; when you plug two devices together, you are indicating that you want them to communicate. But in a wireless link, association is more ambiguous. If a peripheral device wishes to establish a wireless link with a host and more than one host is within range, the peripheral needs some method of determining which host to link with.

Association is also a key element of communications security. Security involves preventing both the unauthorized communications between two devices and a third party's interception of authorized communications. In a wired connection, the need for physical access to the wires provides a high degree of security. It's hard to connect to a host or eavesdrop on wired communications without access to the equipment. The broadcast nature of a wireless link, however, opens the door for both types of activities to occur at a distance.

Encrypting the data stream can provide the needed security. Encrypted data streams are difficult to mimic or to read without possession of the encryption key. Establishing an encrypted data stream, however, first requires a secret exchange of keys between the units. For wireless systems, this exchange occurs during association, with the result that associated devices can communicate with each other, and nonassociated devices cannot.

NEW VERSUS OLD PROTOCOL

The ability to handle security, association, and signal-integrity issues is essential to any wireless-cable-replacement technology. The competing approaches of CableFree USB and Certified Wireless

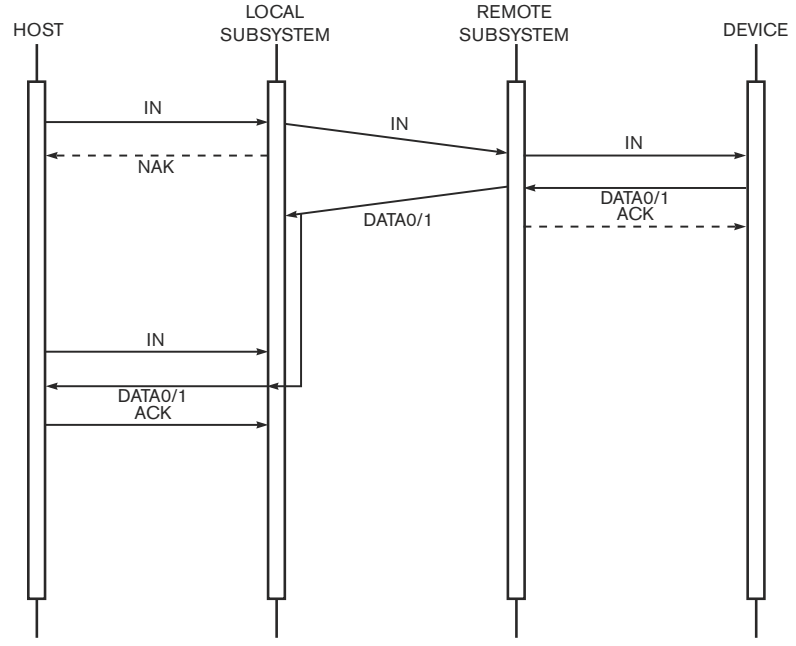

Figure 2 Performing a USB transaction over a wireless link requires that intermediate subsystems work to prevent the USB turnaround timer from creating problems (courtesy Icron Technologies).

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A TALE OF TWO RADIOS

The clash of the wireless-USB standards began as competition for IEEE standardization of personal-area-network-radio technology. To achieve high bandwidth over short distances without creating interference in an already-crowded spectrum, developers turned to UWB (ultrawideband) radio. The conflicts arose in the definition of modulation schemes for the UWB signal.

The UWB radio generates signals that are short bursts—only a few cycles long—of a carrier frequency. The frequency spectrum that results from these short bursts contains many harmonics of similar magnitudes spread out over a bandwidth of several gigahertz. Because the signal energy is distributed across numerous harmonics, the energy at any one frequency is relatively small. This dilution of energy allows a UWB signal to share radio spectrum with more conventional narrowband communications without generating significant interference.

Two modulation schemes for UWB signals arose as contenders for IEEE standardization: DS-UWB (direct-sequence UWB) and OFDM-USB (orthogonal-frequency-division-multiplexing UWB). Proponents of DS-UWB formed the UWB Forum to refine and promote their approach. The supporters of OFDM-UWB created the WiMedia Alliance. For several years, both groups engaged in fierce lobbying within the IEEE-standards process, ending in a stalemate.

The DS-UWB approach has the advantage of simplicity. As Figure A shows, the scheme works on only two frequency bands. A given network uses one band or the other to avoid interference from other networks. Working with only two carriers simplifies the transmitter design.

DS-UWB also employs a simpler modulation scheme. The data stream directly controls the transmitter, turning it on and off with BPSK (binary-phase-shift keying). To prevent repeating data patterns from disturbing the signal's power spectrum, the data stream is first encoded into tokens to prevent such repetitions.

The OFDM-UWB approach is more elaborate, using frequency hopping over multiple channels to avoid interference (Figure B). The scheme allows the transmitter to eliminate noisy channels from the hopping sequence. This scheme also allows multiple networks to operate in close proximity with minimal interference, but the penalty is a more complex and costly transmitter. Proponents of DS-UWB also contend that OFDM performs poorly in the presence of multipath propagation and requires channel manipulation rather than simple pulse shaping to control the output spectrum.

Unable to resolve these conflicting approaches, both camps have now turned to the marketplace for a decision. CableFree USB uses the DS-UWB approach, and the OFDM-USB approach has its home in Certified Wireless USB. Both sides are hoping that their combination of cost, performance, and utility will win the market over.

Recent developments are favoring the OFDM-USB approach, however. The WiMedia Alliance has seen the selection of its scheme by the USB Implementers Forum. In addition, the Bluetooth SIG (Special Interest Group) has now chosen the WiMedia UWB radio as the successor to its current radio scheme. The Alliance has begun to define the behavior of a common radio platform for inclusion in next-generation PCs. With the right combination of protocol-adaptation layers, a single WiMedia radio transceiver can function as a Bluetooth, Certified Wireless USB, FireWire, and TCP/IP (Transfer Control Protocol/Internet Protocol) channel.

The Alliance is also vigorously pursuing worldwide regulatory acceptance of its UWB scheme. The United States allows full use of the WiMedia radio's 14 frequency channels, and other countries are expected to follow suit for many of the channels. In situations in which local regulations restrict channels, however, the WiMedia radio simply removes those channels from the hopping scheme. Thus, a single OFDM-UWB radio design has the potential of achieving worldwide regulatory acceptance. The two-channel DS-UWB scheme now has regulatory approval in only the United States.

Although the outcome of this competition seems to be stacked in favor of the WiMedia approach, it is too early to discount the impact of the design simplicity and early market entry that DS-UWB enjoys. As the market makes its choices over the next few years, it will be the best of times or the worst of times for the two camps. Who will enjoy which is still up in the air.

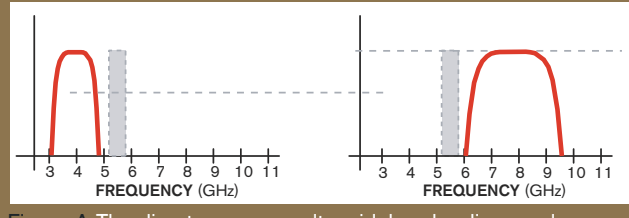

Figure A The direct-sequence ultrawideband radio uses low- and high-frequency bands (left and right, respectively) to avoid interference from adjacent networks.

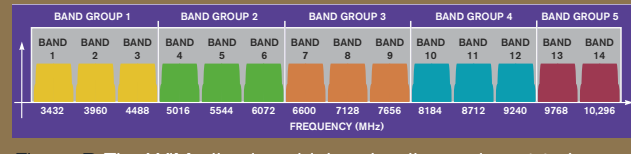

Figure B The WiMedia ultrawideband radio employs 14 channels and uses frequency hopping to mitigate interference.

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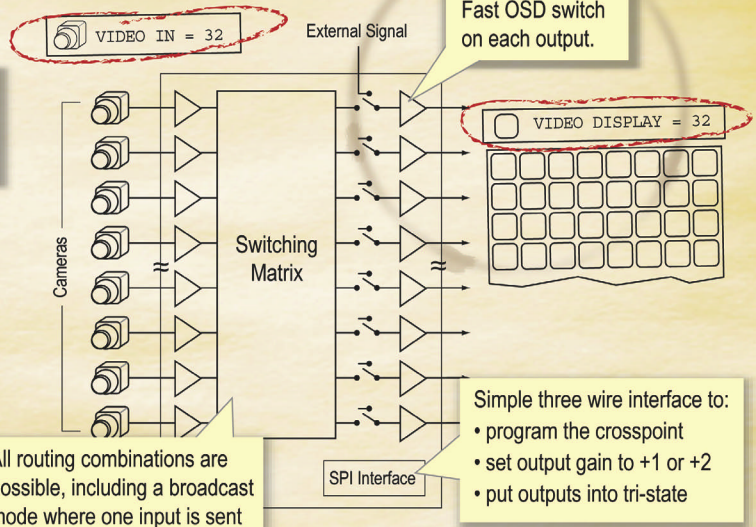

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USB address these issues in different ways. CableFree USB exactly mimics USB 2.0 in its interfaces to host and peripheral devices, handling the wireless issues within device adapters. Certified Wireless USB employs a new communications protocol, similar but not identical to USB, to address the wireless issues.

This first difference in the two approaches could significantly impact their market acceptance. The CableFree approach of retaining the USB 2.0 protocol means that developers can quickly offer products that users can simply plug in without making any system changes. CableFree products, such as the Belkin four-port hub in **Figure 1**, appeared at the Consumer Electronics Show in January. The system offers a hub that connects to the peripheral devices and wirelessly communicates with an adapter, or "dongle," that plugs into the USB port of a laptop computer.

The Certified Wireless approach, on the other hand, required the definition of a new specification. The initial specification, which its developers released in May 2005, received a supplement defining the association's methods in March 2006. The specifications are now under the control of the USB-IF.

Waiting for a new specification has made Certified Wireless USB lag behind CableFree USB in its market introduction, giving CableFree a chance to establish itself as a de facto standard. In addition, introducing a protocol means that implementing Certified Wireless USB involves a software change. This need to change software may further delay implementation, as well as present a barrier to adoption by the market. Such software is beginning to appear, however. Windows XP drivers for Certified Wireless are now available from WiQuest Communications.

The flip side of having a new protocol is that it was developed for wireless communications. This situation has allowed the approach to provide extra value by optimizing data throughput over the radio link and providing power-management features for the radio. These additional attributes bode well for the long-term value of the Certified Wireless approach if the CableFree approach does not first dominate the market.

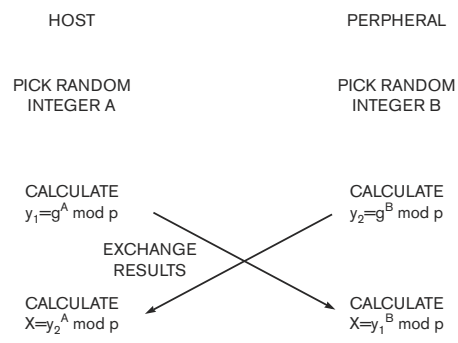

Figure 3 This Diffie-Hellman key agreement protocol is the basis for Certified Wireless USB's unwired-association scheme.

HANDLING SIGNAL DELAYS

The market impact of the two approaches may be important for companies seeking to develop peripherals and host computers, but developers who simply need to use an unwired USB connection will need to look at the technical details to choose the best approach for their application. One of the first places to look is at the signal-integrity issue and its impact on data throughput.

The Certified Wireless USB approach has built into its protocol the features to handle such wireless-channel attributes as noise, fading, and conversion delays. These features add to the protocol overhead, but the USB-IF claims that the protocol has a 75% efficiency in data transfers over a 480-Mbps link. Because USB 2.0 was designed for a wired connection, on the other hand, the CableFree approach requires that you make some accommodation to handle the problems that USB 2.0's turnaround timer causes.

One such accommodation comes from Icron Technologies, developer of the ExtremeUSB extension (**Figure 2**). When the host device initiates a transaction, it expects to receive a response from the peripheral device within the turnaround time. To address that expectation, the ExtremeUSB extension inserts into the link a local and a remote subsystem to mimic the peripheral to the host and mimic the host to the peripheral. When the host initiates a transaction, the local subsystem responds with an NAK (negative acknowledgment), so that the host does not wait for the peripheral's response. The local subsystem then passes the transaction to the remote subsystem, which interacts with the peripheral. The remote subsystem returns the peripheral's response to the local subsystem, which then waits for the host to make a second attempt at initiating the transaction. The local subsystem has the peripheral's response in memory, allowing it to react immediately and complete the transaction.

This approach prevents the delays inherent in the wireless link from slowing the host system's bus. The host need not wait for time-out of the turnaround timer before moving on to the next task. The approach does, however, require that the host make more than one attempt to initiate a transaction before obtaining the desired response. This need for multiple attempts can reduce the effective bandwidth available to the peripheral.

ASSOCIATION METHODS

Another technical difference between the CableFree and the Certified Wireless approaches occurs in the way they handle association and security. CableFree devices have built-in association. The hub and dongle come as a matched pair, with internal registers that contain matching identity information. Communications between the hub and the dongle encapsulate the USB-data packet with a header that indicates the identity of the sender. By first validating the data-packet header, you can then configure the matched hub and dongle to respond only to one another's signals.

This approach prevents outside devices from connecting to the host or the peripheral but does not prevent snooping. The hard-wired identity information, however, can also contain a private key for encryption of the data. Encryption makes the link more costly and complex but provides full data security. A CableFree USB implementation may not have built-in encryption.

The drawback of the hard-wired approach to association is that it prevents the interoperability of devices from different manufacturers. For the home-user

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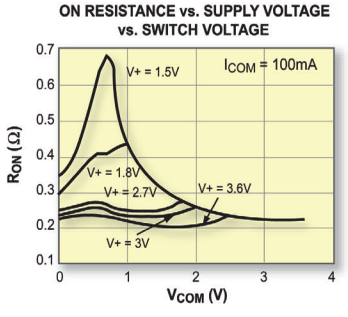
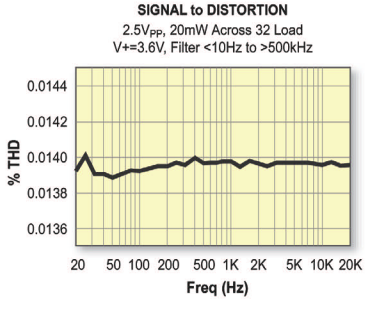
	ISL43L210	SPDT/2:1 Mux	0.44	0.06	6kV	1.1 to 4.5	SC70-6
	ISL43L110	SPST (NO)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
	ISL43L111	SPST (NC)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
Duals	ISL84762	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL84684	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL8484	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 4.5	TDFN, MSOP
	ISL43L220	2xSPDT/2:1 Mux	0.23	0.03	9kV	1.1 to 4.5	TDFN
	ISL43L410	DPDT/Diff 2:1 Mux	0.29	0.03	9kV	1.1 to 4.5	TDFN, MSOP
	ISL43L120	SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L121	SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L122	SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L710	Diff SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L711	Diff SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L712	Diff SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
Quads	ISL83699	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 3.6	QFN, TSSOP
	ISL84780	Dual DPDT/Diff 2:1 Mux	0.45	0.07	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL8499	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 4.5	QFN, TSSOP
	ISL43L420	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.1 to 4.5	QFN
Octals	ISL84781	8:1 Mux	0.41	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL84782	Diff 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL43L840	Dual 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	QFN, TSSOP
	ISL43L841	Diff: 4:1 Mux	0.5	0.056	4kV	1.6 to 4.5	TQFN, TSSOP

ISL84684 Typical Performance





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market that CableFree targets, this characteristic may not be a problem. Home users will adopt CableFree simply to eliminate the need for cables with their equipment. They will not purchase new CableFree peripherals for use with a preconfigured CableFree-ready PC.

The Certified Wireless approach, however, targets next-generation equipment, although, for the home user, vendors are developing a hub-and-dongle approach that can handle legacy USB 2.0. For this next generation, Certified Wireless has adopted association features that will ensure multivendor interoperability and data security. These association approaches allow Certified Wireless to go well beyond legacy installations.

Two methods of association are available in Certified Wireless: wired and unwired. In the wired approach, the peripheral must physically connect through a cable to its target host for first use. Once the devices connect, the user initiates association between them. The host and the peripheral exchange encryption keys and other information across the cable, and then store that information in their internal memories. The two can thereafter automatically establish a secure wireless link without physically reconnecting. The host keeps a record of all peripherals that it has associated with. The peripheral must retain association data on at least one host but may have enough memory to remember several hosts.

UNWIRED-DISPLAY NEEDS

The unwired-association method, or numeric model, uses the Diffie-Hellman key agreement protocol to establish a secure channel. The method depends on a user's reading a two-digit display on each device to verify that the association is correct and then signaling each device to accept the association. This display requirement adds cost to the devices, but, because the approach targets devices that may have displays, such as printers and cameras, this constraint may not matter.

The Diffie-Hellman protocol has three elements (**Figure 3**). The first element is a pair of numbers, g and p, that are publicly known. The number p is a large prime, and g is an integer less than p. The

THE UNWIRED-ASSOCIATION METHOD, OR NUMERIC MODEL, USES THE DIFFIE-HELLMAN KEY AGREEMENT PROTOCOL TO ESTABLISH A SECURE CHANNEL.

second element is the ability for the host and peripheral to independently develop random numbers. The third element is the ability of the host and peripheral to perform calculations of the type $y=g^X$ mod p, where mod means to use modulo arithmetic.

The protocol offers a secure way of exchanging keys. When the two devices attempt to associate, each generates a random number: A for the host and B for the peripheral. The host then calculates: $y_1=g^A$ mod p, and the peripheral calculates: $y_2=g^B$ mod p.

The devices exchange their results, and then use them to calculate $X=y_1^B$ mod p (peripheral) or $X=y_2^A$ mod p (host). This calculation yields the same number in each device, $X=g^{AB}$ mod p without revealing the random numbers.

To complete the association process, the user must verify that the two devices have reached an agreement. The devices each display a two-digit contraction of the result for X, which the user compares and verifies. The value g^{AB} becomes a shared secret key for the two to use in further communications. Because the system chooses a new random number each time it makes an association, only the two devices involved have possession of their private key. As with the wired approach, the host and peripheral must keep track of the keys and other data generated during the association.

The advantage of the Certified Wireless association method is that it allows devices from different manufacturers to associate at will, which, in turn, allows computers and other devices to build in support for Certified Wireless without knowing which devices it is will associate with. Certified Wireless thus becomes a cable-free replacement for USB functions rather than a simple replacement for a single USB cable.

All of the complexity associated with the new protocols of Certified Wireless USB may make the approach unsuitable for some applications. For those applications, the simpler and less expensive approach that CableFree USB offers can be compelling. Still, the long-term fate of the two approaches remains uncertain.

History has shown that being first in the market, like CableFree USB, can be a compelling advantage regardless of technical attributes. At the same time, the Certified Wireless approach has the backing of the USB-IF as well as industry powerhouses, and it promises both high performance and multivendor interoperability. One set of advantages may overwhelm the other, or both approaches may find a home in noncompeting applications. Deciding which approach to adopt will determine the outcome in this clash of the wireless-USB standards. **EDN**

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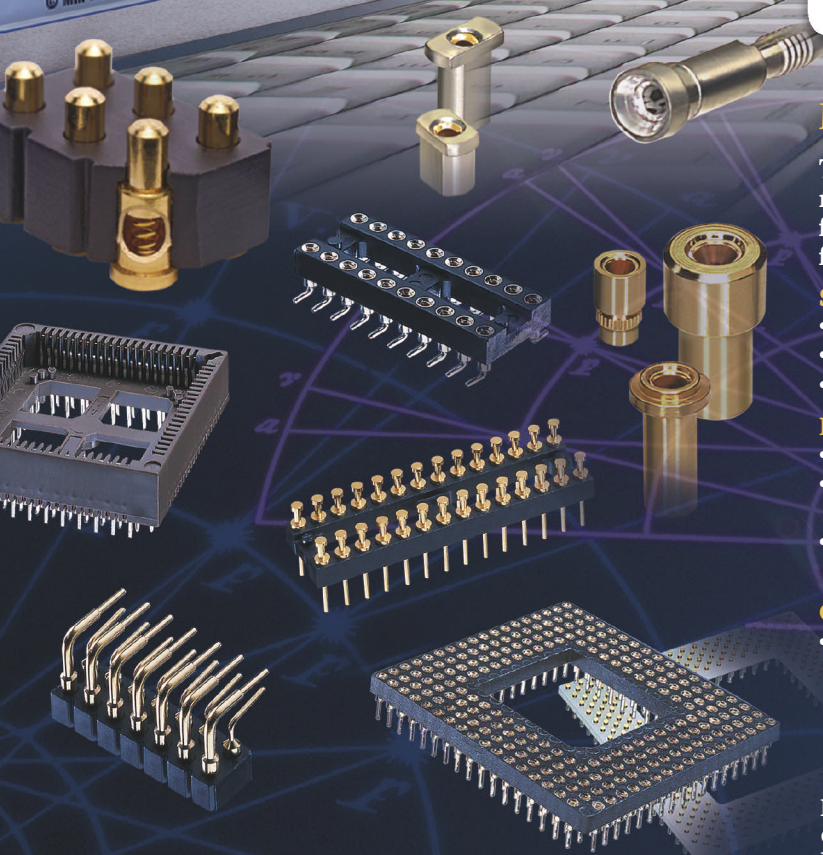

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THE RIGHT VIDEO ARCHITECTURE

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BY RON WILSON • EXECUTIVE EDITOR

Video is going handheld.

DIGITAL-VIDEO BROADCAST AND THE IPOD PHENOMENON HAVE IGNITED A RACE TO BRING VIDEO TO THE PALMTOP. PROCESSING ARCHITECTURES ARE AT THE CENTER OF THE STRUGGLE.

Consumer-electronics manufacturers are rushing past handheld DVD players to compete against the Video iPod. Handheld receivers for the emerging DVB (digital-video-broadcast) standards are on everyone's drawing boards. Video approaching VGA (video-graphics-array) resolution is flickering to life in cell-phone handsets. And in every one of these markets, the most forward-looking pundits are predicting the arrival of high-definition handheld devices.

All of this could be an obvious boon to consumer-electronics and handset manufacturers, persuading consumers to rush out and buy another multihundred-dollar toy and again replace their cell phone while they are at it. But the growing demand for decent video on handheld devices is posing a serious challenge to system designers, and it is confronting system architects with a too-large menu of hard choices.

THE OEM'S DILEMMA

The first decision an end-system designer must face is how much work to do. In many of these markets, you can license a complete system design, including the user-interface software, board film, and enclosures, and simply arrange to have an OEM manufacture it. That approach involves minimal development cost, but the only opportunity for differentiation is a clever choice of a reference-design vendor. At the other extreme, you can start with IP (intellectual-property) cores and design an SOC (system on chip), design a board, select peripherals, and create the system from an almost-clean sheet of paper. This approach offers the greatest opportunity for differentiation—without any guarantees of success unless your organization happens to have deep expertise in digital-video processing—but it could take 50 man-years.

"Customers today aren't looking for reference designs as much as they are looking for complete solutions," says Josh Kablotsky, engineering fellow at Analog Devices Inc. "They want to push all the complexity back onto their vendors, but, at the same time, they want the ability to differentiate."

It is an understandable position. The connections between algorithms, system resources, and the end-user experience are highly complex and have their roots in the deepest levels of system implementation—both hardware and software. Except for a handful of vendors that have long experience in digital-video systems, much of the expertise is inaccessible. It makes sense to ask semiconductor suppliers—which have attempted to position themselves as experts—to solve these problems.

But this stance has profound implications for both the system vendors and the semiconductor vendors. For the systems vendors, it means they must accept the design of their device as a black box, with only a few design knobs and a promised road map on which to build a market position. They must be able to estimate from demos and superficial descriptions just how far they can turn the knobs and in just which direction the road map is likely to turn.

For the semiconductor vendors, the growing importance of the reference design means that their cherished architecture—often the crown jewel of a senior design team—is all but irrelevant to the customer. "Customers just want a solution to their problem. They don't make choices based on architecture," Kablotsky says. The predicament also means that, to play in these markets, a vendor must provide a complete product, including hardware, codecs, application software, operating systems, and user-interface tools. The primary products customers will get from semiconductor vendors are the APIs (application-programming interfaces) of the software modules, not the underlying hardware. Architecture indirectly becomes an issue in system design depending on the chip developer's ability to attract software partners and to provide powerful APIs.

THE SOPHISTICATED OEM

A look inside a sophisticated OEM provides an illustration of this delicate balancing act. Fast Forward Video has been building JPEG-based digital-

AT A GLANCE

- Handheld devices that can decode and display broadcast or even high-definition video are promising target markets for chip and system developers.
- Designers will build most handheld-video systems from chip vendors' complete reference designs, and the system OEMs may know little of the underlying architecture.
- Improvements in CPU and DSP energy efficiency are allowing chips to compete alongside traditional hard-wired approaches to video codecs for these applications.
- Designers use a mix of programmable and hard-wired blocks, but many agree that significant hardware support for advanced video codecs will be necessary for high-definition TV.

video-recording subsystems since 1999. The company designs at the board level, eschewing FPGAs or ASICs in favor of standard-product ICs whenever possible. The company differentiates itself not with custom hardware but with substantial expertise in video-processing algorithms.

This approach is no mean trick when you're performing it on someone else's chip. "The No. 1 issue is keeping the flow of data between the outside world and the disk drive unimpeded," explains Fast Forward's president, Paul DeKeyser. This issue forces the company to delve into the internals of any JPEG hardware it evaluates. "The second is to have the right codec for the desired results." This need dictates that the company must use JPEG-2000 codecs. "Any scheme that uses intraframe encoding has image problems unless you can do multipass encoding," DeKeyser observes.

One of the greatest difficulties is matching the highly variable data rates into and out of the codecs to the plodding but sporadic pace of the disk drive. "We started out with an LSI Logic chip set," says DeKeyser. "It did JPEG, but the data rate was so highly variable that we had to buffer it." Now, the company uses Zoran chips. "With JPEG-2000, we have the concept of metered data rates; the chip keeps track of a target data rate and works to keep its average close to the target. That is one of the strengths that attracted us to Zoran's chips," he says.

Fast Forward's knowledge of the chip has become intimate, reaching into parts of the JPEG engine that many users may not realize are user-programmable. To balance data rate against subjective image quality, the company experiments with such innards as Huffman-coding tables, for example. "This becomes a sort of tribal knowledge—what register settings will work best for a particular chip," says DeKeyser. But extracting this kind of knowledge takes experience. And that experience is unavailable at the beginning of a design, when chip selection must happen. So, a design team must be able to "tease an evaluation out of a demo," as DeKeyser puts it. This situation is so even if a demo looks terrible because the chip vendor doesn't understand the importance of data converters or looks wonderful because the vendor has tuned it around one sample bit stream. The design team must estimate not only the quality of a chip, but also how far team members can accurately optimize the chip before the architecture runs out of steam. It takes intuition and communication with other people in the close-knit video community who have used the chip. "We would never use a brand-new device," DeKeyser declares.

LEVELS OF ABSTRACTION

With customers varying from those who want a turnkey system to those, like Fast Forward, who manipulate hardware registers, silicon vendors face having to provide not only full systems built on their chips, but also multiple levels of

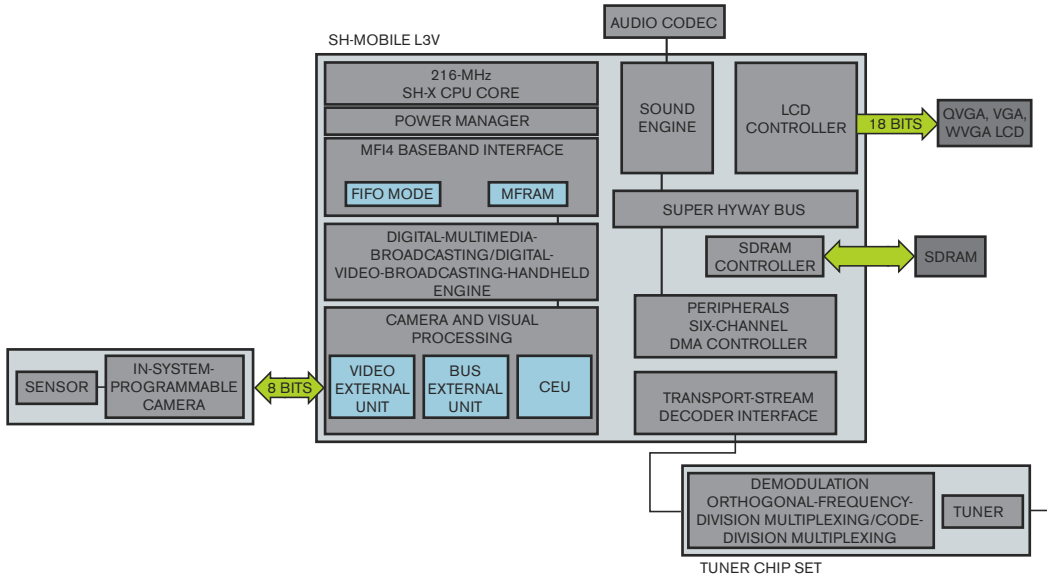

Figure 1 Renesas surrounded an SH CPU/DSP core with big, hard-wired video processors to achieve its price/performance target for mobile-video receivers.

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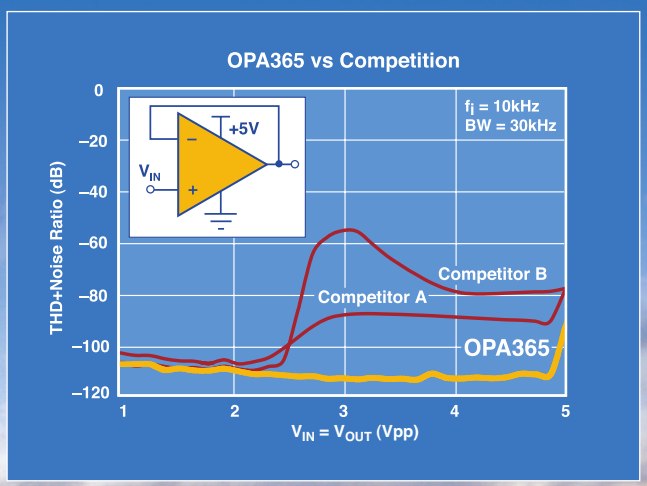

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access to these reference designs. Some users may see the reference design as a complete system and want access only to the user interface. Others may see the platform as a collection of APIs running on a host CPU, perhaps complying with the Khronos Group's OpenMax royalty-free, cross-platform API, so that they can add or remove codecs in a standard way. Still others may want to understand the fine structure of application and codec tasks so they can, for instance, manipulate codec parameters or reorganize data flows to and from DRAM. And others, like Fast Forward, may want to understand the operation of individual hardware blocks at a register level. This diversity of needs can create mind-bending customer-support and design-update issues for a vendor, especially if it relies primarily on partners for codecs and applications. A silicon vendor may find itself counseling a customer on optimizing a codec that a third party in another country wrote.

The viability of providing different levels of access to a reference design, the effectiveness with which the user can manipulate the design, and the range over which they can configure the design are all functions of the underlying architecture. Some architectures target one specific market and are impractical for any other use. Some attempt to balance two mutually antagonistic goals—flexibility and efficiency—covering a range of end products with a single hardware platform. And others make strong commitments to flexibility and scalability, even at the expense of energy efficiency and cost.

THE RIFLE SHOT

Some markets are large and stable enough that it makes sense to offer SOC designs just for them. The emergence of mobile-video-broadcast standards in some Asian markets is a case in point. Renesas recently announced the CPU-centric SH-MobileL3V SOC, which finds use as a handset application processor in DVB applications (**Figure 1**). According to Brian Davis, director of business development at Renesas, the device uses the SH-X processor core, which in turn is based on the superscalar SH-4. The SH-X adds a DSP subsystem to handle audio codecs in software. Even though the SOC targets mobile television in just two geographic markets, the range of audio codecs in use even within this narrow space still demands a software approach, according to Davis. The SH-X provides more than enough head room for an operating system, application code, and software-audio codecs.

In contrast, Renesas judged that a pure-

AN ARCHITECTURE FOR AGILE RICH-MEDIA PLATFORMS

By Iole Moccagatta, Vincent Nollet, and J-Y Mignolet, IMEC

The digitalization of electronics enables the convergence of high-quality multimedia services with high-speed data communication. This combination should offer ubiquitous access to the Internet and anywhere and anytime usage of services, content, and applications. Consumers should be able to access services and information while at home, walking in urban areas, driving a car, and even in remote, rural locations. To support all these scenarios, mobile terminals should be able to support and seamlessly switch between WLAN 802.11n, 3G/4G, 802.16e, and DVB-H (digital-video-broadcast-handheld) communications standards and MPEG-2, MPEG-4, AVC/H.264, and MPEG SVC (scalable-video-coding) content formats. IMEC is developing the necessary technologies to make this scenario happen.

Designers must overcome some major technological roadblocks before they can develop a multimode, multimedia terminal that supports these scenarios. These roadblocks include the increasing complexity of multimedia encoders and decoders, the need for a seamless switching mode across communication standards, the increasing device cost and power consumption that these terminals require, and the need for fast time to market.

In its M4 program, IMEC develops the building blocks that address these technical challenges. These blocks include a software-defined-radio front end and digital baseband, a 3MF (multimedia-multiformat) codec, and a quality-of-experience manager.

The M4 terminal's 3MF codec should support audio- and video-compression and 3-D-graphics standards. Toward that end, IMEC has developed a flexible, heterogeneous platform that can support current and emerging video- and audio-compression standards. The company plans to demonstrate a power-efficient implementation of the emerging MPEG SVC standard on such a platform. SVC, currently in the last stage of the MPEG-standardization process, aims for highly efficient compression by combining the ITU (International Telecommunications Union)-TH.264/MPEG AVC (advanced-video coding) with embedded-content scalability. Content scalability is the key for coping with instantaneous variations in usage conditions, such as platform-resource usage, communication bandwidth, and transmission errors, which typically occur in the M4 context, and preserving the quality of the user experience. The combination of high compression performance and embedded-content scalability, however, comes at the cost of an order of magnitude higher complexity. The challenge is thus how to achieve cost-efficient, low-power implementations of SVC on a flexible platform.

During the past year, IMEC has defined a platform meeting these requirements. It comprises multiple IMEC ADRES (architecture-for-dynamically-reconfigurable-embedded-systems) processors in a multiprocessor configuration and third-party components. The platform also contains a scratch-pad-based data-memory hierarchy, and each ADRES processor has its own advanced DMA controller to access this hierarchy.

The ADRES processor features a core that com-

hardware approach was feasible for video because the device needed to support only the MPEG-4 and H.264 video profiles. It also deemed a software approach to video decoders and still-image codecs to be prohibitively damaging to battery life. Hence, the design clusters hardware blocks for video, still-camera processing, and peripheral control around the CPU, and the proprietary Super Hyway silicon bus interconnects them. "The video decoders are implemented in hardware that is like a series of state machines with built-in math functions," Davis explains. "There are enough similar functions between MPEG-4 and H.264 that, with careful design, they can share some of the state machines. And our studies show that, with additional host software, we can cover Windows VC-1 using the same blocks."

Relying primarily on hardware gives Renesas significant energy efficiency. Power numbers are notoriously difficult to compare because so many parameters can have a first-order impact on energy consumption. For instance, does a given power figure include video scaling and color-space conversion? Does it include the display drivers? According to Davis, the SOC can perform the audio/video-decoding and display-preparation jobs in CIF (common-intermediate-format) resolution at approximately 200 mW.

Renesas exposes this architecture to customers at two levels. In Japan, the chip, which now serves as the basis of a merged application/baseband design with NTT, is available as a complete reference design. In Korea, in contrast, Renesas works with system-integration partners to tailor the reference design to local needs.

There can be many variations on this theme. Qualcomm, for example, has approached a similar problem—a line of cellular handsets with video-gaming capability—with its own set of CPU-plus-hardware architectures. But, unlike Renesas, which aimed a chip at a narrow range of markets, Qualcomm designed one SOC for each price and performance point in the handset-gaming market. "Ideally, at different performance levels, you would make different architectural trade-offs," explains Dave Ligon, senior product manager at the handset giant. "We divide this market into three segments: the multimedia phone, which is primarily cost-sensitive; the enhanced phone; and the convergence platform, in which the gaming requirements are stringent."

Qualcomm's chosen architectures directly reflect these three segments. The multimedia phone, for example, implements the platform's application-DSP core for geometry processing and an

prises a coarse-grained, reconfigurable array and a tightly coupled VLIW (very-long-instruction-word) processor. The core is fully programmable from C, thanks to the co-developed C-code compiler. It beats the performance of state-of-the-art DSPs by offering the same flexibility plus the power efficiency of state-of-the-art ASIPs (application-specific instruction processors). For a 32-bit ADRES core with eight-by-eight functional units in a 90-nm CMOS technology, the processor's power efficiency ranges from 50 to 70 million operations/sec-mW, and peak performance is approximately 25 billion operations/sec at 400 MHz. The device occupies approximately 7 mm², including the core and the L1 cache. The cache includes 32 kbytes for data, 128 kbytes for instruction, and 16 kbytes for configuration memory.

An innovative, multiprocessor SOC (system-on-chip) application-mapping design flow supports application development. This flow employs IMEC's proprietary, leading-edge design tools, such as Sprint to create parallelism and Atomium to optimize the memory hierarchy and minimize the number of memory accesses. These tools enable mapping an application onto a platform containing multiple heterogeneous, flexible processing units–in this case, the ADRES core–that interconnect through a network on a chip. The application-mapping tools also enable easy use of intelligent DMA controllers, such as the ADRES DMA controller, to manage the memory hierarchy and to optimize the data transfers.

Because of its flexibility, this platform can support a variety of video codecs, offering the advantage of easy scalability toward a range of multimedia applications and thus a low cost of ownership (Figure A). For example, the platform supports scalability by allowing users to turn off processing units when they are not in use. Operating at maximum performance, the platform should dissipate less than 700 mW in a 90-nm, 1V implementation. The platform can support H.264/AVC decoding to high-definition-TV resolutions with rates of 30 frames/sec and SVC decoding to VGA resolutions with rates of 30 frames/sec.

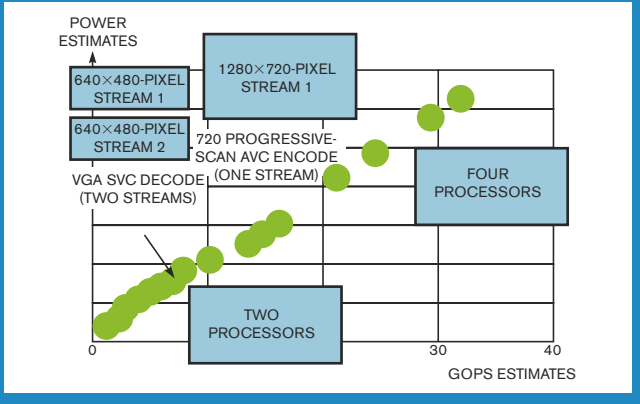


Figure A Increasing the number of ADRES processors smoothly scales performance of the platform.

AUTHORS' BIOGRAPHIES

Iole Moccagatta, PhD; Vincent Nollet; and J-Y Mignolet work in the DESICS (design-technology-for-integrated-information-and-communications) division of IMEC (Interuniversity MicroElectronics Center, Leuven, Belgium).

ARM core for software-based rasterization. Using lots of properly organized local memory makes the performance goals achievable at this level.

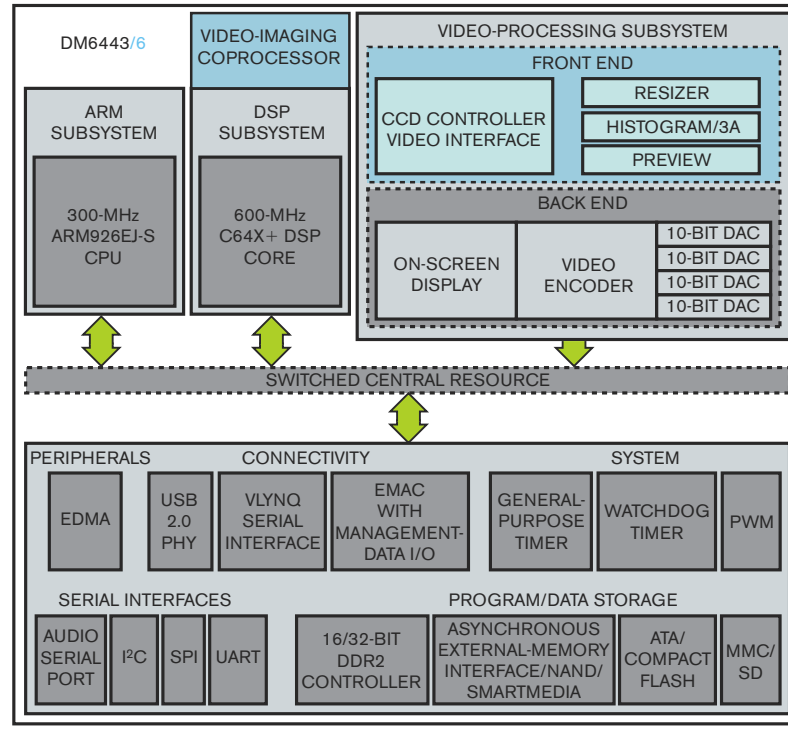
The enhanced platform employs hardware rasterization. A z-buffer, along with other hardware-based early-exit strategies, ensures that only visible pixels pass through the pipeline. The geometry-DSP cores connect directly to the rasterization engine to eliminate the energy that a bus or a shared-memory approach would consume. The raster engine, in turn, drives a mobile-display processor that, in addition to creating signals for a small LCD, implements simple 2-D operations.

At the high end, the convergence platform employs a derivative of the ATI 2300 graphics core in combination with an enhanced version of the mobile-display processor. "The convergence platform gives a bit higher graphics performance than the Silicon Graphics Octane workstation that was the current hot product when I worked at Silicon Graphics," Ligon says. "And this is a single system in package in a handset."

In practice, the graphics APIs largely conceal the significant hardware differences among the three platforms, so game developers can almost regard the three as one platform, he says. As it moves up the product line, an OEM would see additional features but no fundamental changes in software interfaces. This approach can offer the ultimate in energy efficiency over a range of tasks. But, as Qualcomm's three distinct chips indicate, flexibility means the need for additional chip designs. For a cash-rich company with intimate customer relationships that make it confident of hitting a huge market, that trade-off is a good one. But not everyone is in that situation.

ADDING PROGRAMMABILITY

There is a natural evolution from a purely CPU-centric architecture in which hard-wired engines surround a single programmable core to a more flexible architecture in which the specialized engines themselves become programmable. Some current thinking that went into Texas Instruments' DaVinci platform illustrates this first step (**Figure 2**). "There are places for hard-wired blocks and places for programmable blocks," observes



NOTE: ■ = DM6446.

Figure 2 TI's DaVinci approach combines a CPU, a separate DSP core, and a blend of register-configurable and programmable blocks as necessary to reach its goals.

TI fellow Ray Simar. "It's important not to start with a preconceived notion of architecture but to start with an understanding of the application's requirements and how they will evolve over time. Then, think about architectures."

The cost of adding some level of programmability to functional blocks has been slowly edging down. "Power has been getting to be a harder problem for everyone," Simar says. "But with aggressive power-management techniques and careful memory architecture, the energy consumption of a programmable block may be getting closer to that of a hard-wired block."

Simar also points out that a spectrum of programmability occurs within blocks, depending on the granularity of the computation and the number of modes in which the block must function. In some cases—motion-estimation search and compare, for example—an operation is so close to a fixed data-flow model that register-programmed state machines can cover all the application's needs. In other cases, so many variations on an operation may exist or a function may be so data-dependent that only a device with stored programs and a program counter can be flexible enough to keep up. TI has employed the whole range of options beside its DSP cores.

One function that many designers think of as fixed but that is increasingly demanding programmability is DMA. Data movement within a multimedia subsystem can be highly complex, data-dependent, and variable. Simply routing data blocks into and out of DRAM would in many cases result in catastrophe. TI attacks this problem with a combination of embedded SRAMs, which are large enough to hold a full working set for the function the block performs; flow-through architectures when possible; and programmable-DMA controllers to match DRAM-traffic patterns with the needs of both functional blocks and DDR DRAMs.

PEER MULTIPROCESSING

The same style of analysis—beginning with use cases, identifying tasks, and partitioning them into hard, configurable, or software-driven blocks—can lead archi-

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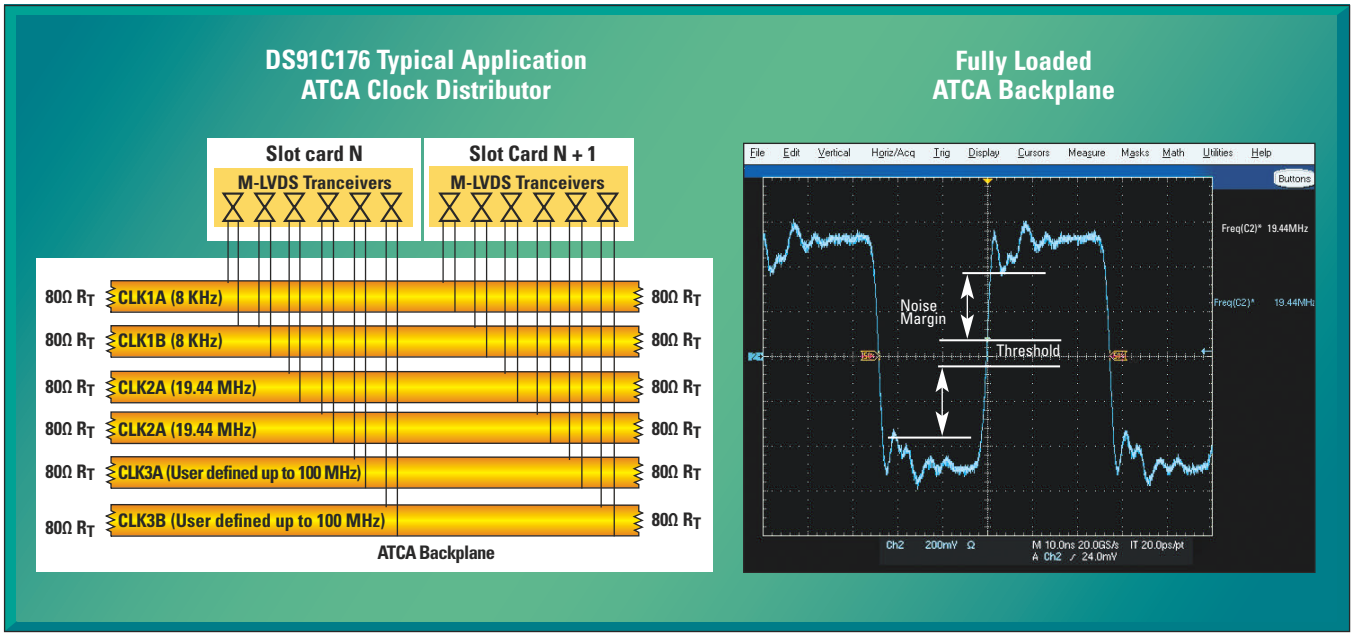

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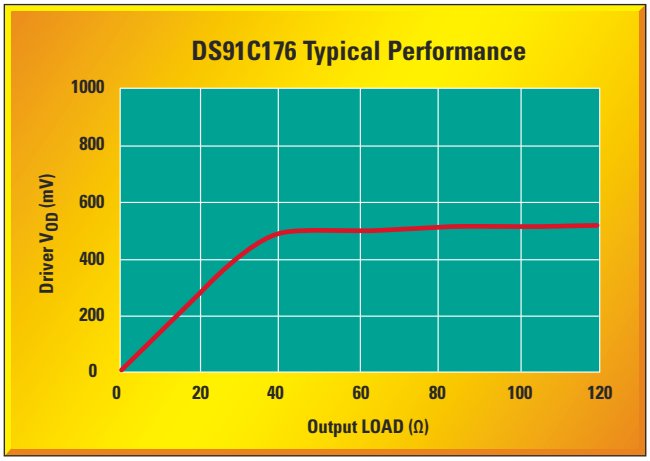

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tects to different conclusions. Nvidia's GoForce product line, for example, has hard-wired engines, but the bulk of the work falls upon Tensilica-derived programmable-DSP cores with enhanced instruction sets. The DSP cores themselves repeat the same pattern in microcosm; Nvidia implements the instruction enhancements in fixed hardware.

"You have to be very clever about what goes into hardware," says Geoff Ballew, Nvidia's director of product marketing. On the one hand, fixed hardware delivers the best energy efficiency—better than the augmented DSP blocks and far better than a conventional DSP core. On the other hand, you'd better choose wisely. Sometimes, with a little more work, you can reuse a block that appears to be fixed-function across a number of codecs, for instance.

Part of the problem is that no good tools exist for energy profiling at the system level. It's a challenge to identify which blocks will be the major energy consumers. Once you identify those blocks, Nvidia further decomposes them and employs dynamic, fine-grained clock gating to switch on and off groups of circuits within the block, minimizing energy consumption.

Deciding how much flexibility you need is difficult, according to Steve Barlow, senior director of engineering at Broadcom. At resolutions below CIF—or D1 resolution in a 65-nm process—for example, you can acceptably deal with most functions in programmable hardware. Above that level—as the functions of set-top boxes begin to converge with those of mobile-video devices, for example—hard-wired engines become necessary. Broadcom's approach is in many ways similar to Nvidia's: programmable processors enhanced with special hardware. In Broadcom's case, the processor is a proprietary CPU core with a 16-element vector processor and a 2-D register file, which Broadcom acquisition Alpha Mosaic developed. This architecture was sufficiently robust to allow a single chip design to support MPEG-4 and, with only software changes, adapt to the demand for H.264. But for set-top-box levels of performance, Broadcom needs to augment architecture with more fixed-hardware blocks. "There are some functions, such as the CABAC [context-adaptive-binary-arithmetic-coding] function in the H.264 main profile that simply don't map well onto vector hardware. At some point, you are up against the limit of what semiconductor technology can do, and you have to go hard-wired," says Barrow.

ABSORBING THE FUNCTIONS

In an interesting bit of evolution, some multimedia architectures have picked up this concept of hard-wired functions within a DSP core and used them not to build specialized blocks, but to build a single powerful DSP core that can itself handle all the media tasks in a handheld system. This approach relies on careful study of the algorithms necessary for video processing, identification of the hot spots within those algorithms, and development of instruction-set extensions to break up the hot spots.

"Applying systems expertise to crafting the microarchitecture of the DSP core can give anywhere from double to 20 times the performance on these algorithms," says Analog Devices' Kablotsky. And that performance is enough to handle, for example, CIF-level H.264 decoding entirely in the Blackfin DSP core with about 20-mW power consumption. However, centering computationally intensive tasks on the DSP core invites two problems: It increases the number of instruction fetches, or the amount of wasted energy, necessary to complete the tasks, and it increases the core-clock rate, again increasing energy consumption. Kablotsky argues that creating instructions tailored to the algorithms helps both of these issues. By combining large numbers of operations—the entirety of an inner loop, for example—into a single new instruction, you can reduce the number of required fetches. By developing extensions to the microarchitecture to exploit data-level parallelism through the use of SIMD (single-instruction-multiple-data) instructions, for example, you can slash the clock rate.

DSP licenser Ceva has taken a similar

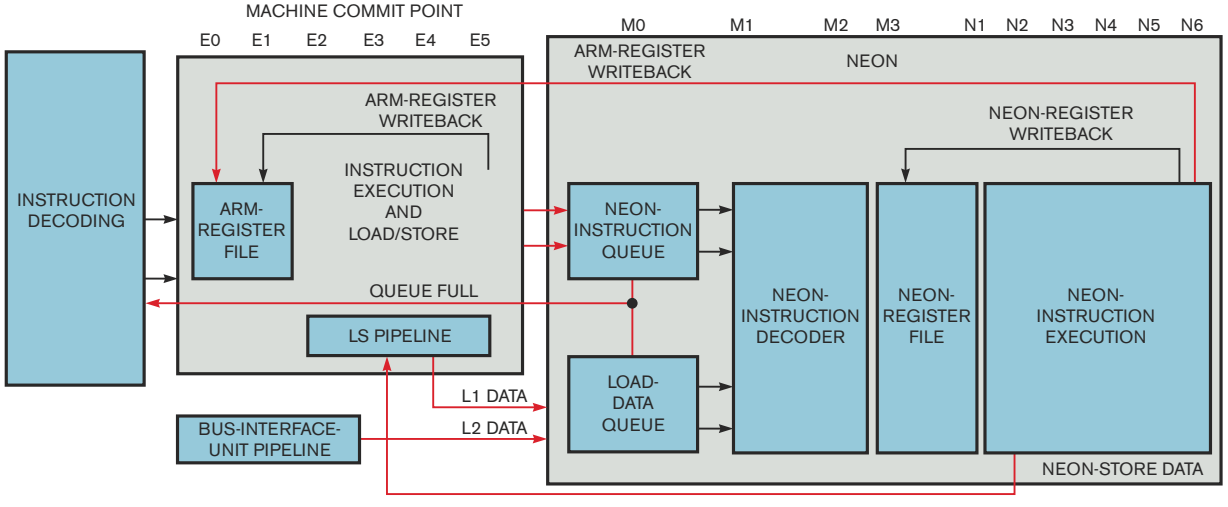

Figure 3 To achieve efficiencies, the Neon SIMD processor in the Cortex A8 architecture stitches intimately into the Cortex CPU pipelines.

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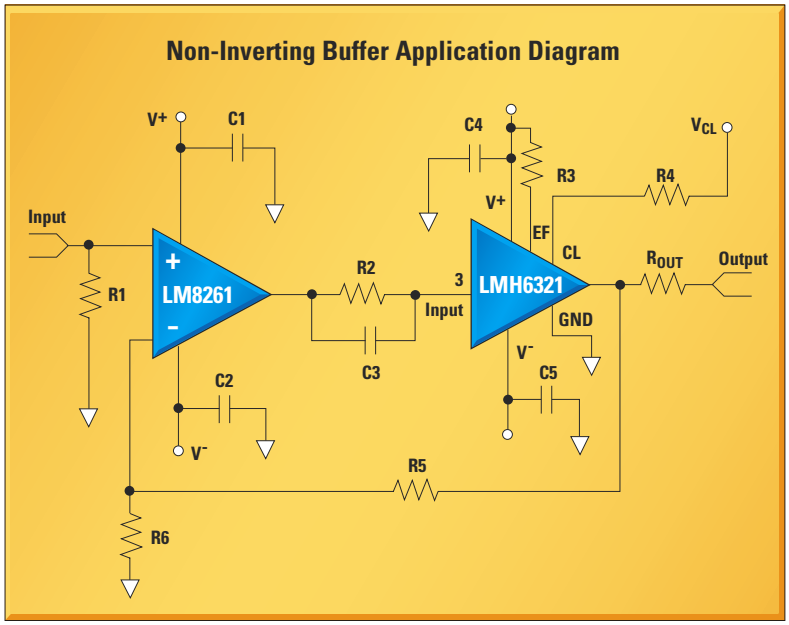

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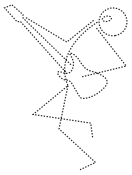

approach. In this case, Ceva based the microarchitecture evolution on an acquisition that brought the company ownership of the FST (fast-subspace-tracking) algorithms for video processing. According to Ceva's vice president of sales, Issachar Ohana, the FST software dramatically speeds video operations. By incorporating instruction extensions for the FST code, Ceva developed the CevaX core, which Ohana claims can perform 30-frame/sec H.264 decoding at resolutions as high as D1 without external hardware assistance. "The combination of these algorithms and the tuning of the core to execute them give us energy consumption competitive with that of hardware," he says.

Having all the computation flowing through a single DSP core simplifies things. But the big advantage, according to Kablotsky, is that it presents a single, C-level-programming model to developers. It presents all the features that a system OEM might want to customize and all the hooks a codec developer or highly skilled video house might want to tweak as source code for a microarchitecture. This approach eases both modification and extension of the system architecture, at least within the range of the DSP's computing power and the battery-life tolerance of the user.

A third example comes from the opposite end of the processing-core world: ARM. Keith Clarke, vice president of technology marketing at the CPU giant, walked through the evolution of the single CPU as multimedia processor. The ARM7 by itself is adequate for some audio applications. But add the 16-bit saturating arithmetic instructions and increased speed of the ARM9, and you get not just audio, but also MPEG-4 QCIF (quarter-CIF) encoding at 15 frames/sec at approximately 80 MHz. Add speed and the SIMD instructions of the V6 instruction-set architecture on the ARM11, and you can achieve VGA-resolution H.264 encoding. Move one step further to the Cortex A8 and the Neon accelerator with its 64-bit SIMD architecture (**Figure 3**), and you can perform 30-frame/sec MPEG-4, VGA encoding in about half the cycles that the ARM11 would require. That task in real time requires about 300 MHz. To make these options more realizable to users, ARM is now prototyping a parallelizing compiler that can extract data parallelism and employ the SIMD hardware to exploit it.

GOING MULTICORE

A highly optimized central DSP or CPU core is not necessarily the end of the road. Analog Devices, ARM, and Ceva all suggest that multiple cores might be necessary for the multiple high-definition data streams in set-top boxes, for example. Other vendors, such as Cradle Technologies, are also looking at a multicore approach based on customized DSPs. The company offers an asymmetric cluster of fully programmable DSP cores that reside around a shared central memory. Having the right extensions on the right DSP core and providing that core's local memory with the right data becomes the essence of system architecture. Designers with an intimate understanding of both

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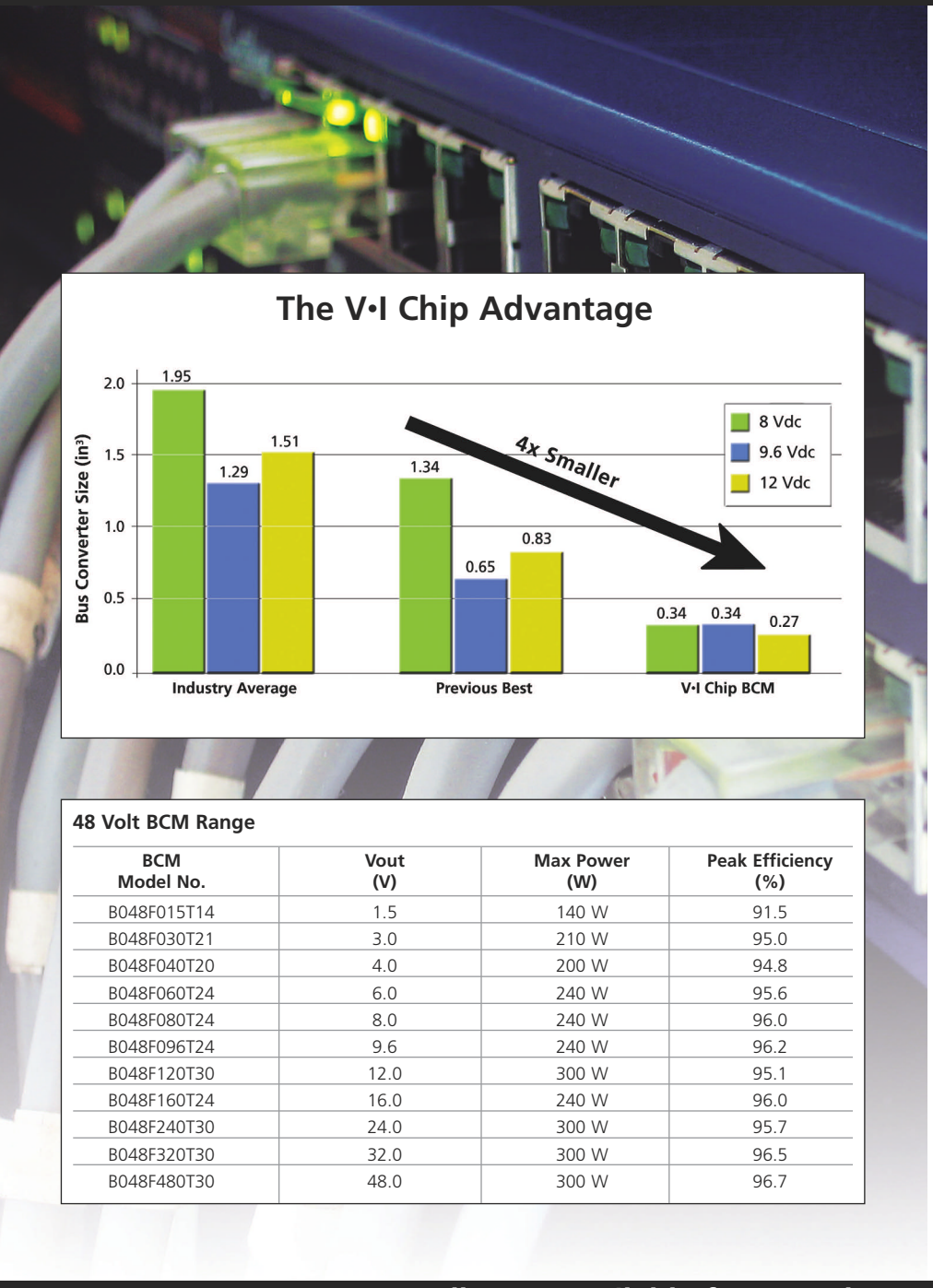

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the use scenarios and the algorithms must make all these decisions, according to Cradle's vice president of applications, Bruce Schulman.

According to Schulman, one critical step is to partition the application into large enough blocks. If too little processing takes place in each block, too much traffic will pass through the shared on-chip memory, and system throughput will suffer. If too much processing takes place in each block, the chip will be unable to exploit the inherent task of parallelism in the application. Another critical step is to study the flow of data through functional blocks and conduct prefetching under program control so that a computing block is never waiting for data and so that the chip efficiently uses external DRAM.

All of these features give the architecture significant flexibility across a range of systems with similar applications. However, only the stout of heart will undertake programming the individual DSP cores. For the most part, customers relate to the Cradle architecture through its APIs.

A SYSTEMATIC APPROACH

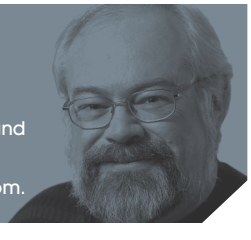
These architectures represent the best analyses of their designers, plus a lot of vested interest, institutional inertia, and tradition. Vendors tend to start with the architectural biases that made them rich in the first place. Yet, from the tremendous variety, patterns emerge that suggest that a systematic approach to video-rich-multimedia architectural design is possible. Any such approach would start with an intimate relationship with the codec and application developers, whether they are in-house or third party. Without this knowledge, you can't accomplish much. With it, system architects can begin with a task-level model of the system, complete with the data flows for expected use patterns.

From this model, the architects should first extract the computational or data-moving hot spots—those code sequences that will consume the most time, energy, or both. Using conventional approaches such as pipelining, SIMD engines, and state machines, designers can tame these hot spots with dedicated hardware. These accelerators can just stay on paper for the moment; designers need not implement them in any particular fashion, but they reduce the estimated execution times and energy consumptions of the code sequences they accelerate.

Next, architects can partition the overall tasks into large blocks in such a way that the overall system requires minimum bandwidth between blocks. Motion estimation or Huffman decoding, for example, might be blocks. This step is vital: In today's technology, computation doesn't cost much, but bandwidth feasts on energy. When you have identified all the blocks, you can organize them based on the data flows and decide which ones you can string into pipelines, which you can arrange in parallel, and which are stubbornly sequential.

You then group the blocks, along with the accelerators you created for them, and map them onto the fewest processing sites that can meet both the throughput and the energy requirements of the system. If one mighty ARM core with a number of extended instructions can do the job at an acceptable clock frequency, you're done. If it requires a dozen little DSPs, each with its own accelerator, so be it. The idea is to map the blocks onto the smallest amount of computational resource necessary. If you have the time, you can now perform an optimization step, looking at all the accelerators that happen to land on each processing site to see whether they can share hardware without resource contention. If so, you might merge two or more accelerators into one slightly more flexible one. Finally, you outfit these processing sites, whether they are CPUs, DSPs, or blocks of dedicated hardware, with local memory and connect them to each other and to central DRAM in whatever manner is necessary to meet the required data-flow bandwidth.

Although no one is likely using this explicit approach, it organizes and describes the tangle of individual decisions that make up a multimedia architect's job, and it explains the blossoming garden of architectures that is rapidly appearing in the handheld-rich-video market. EDN



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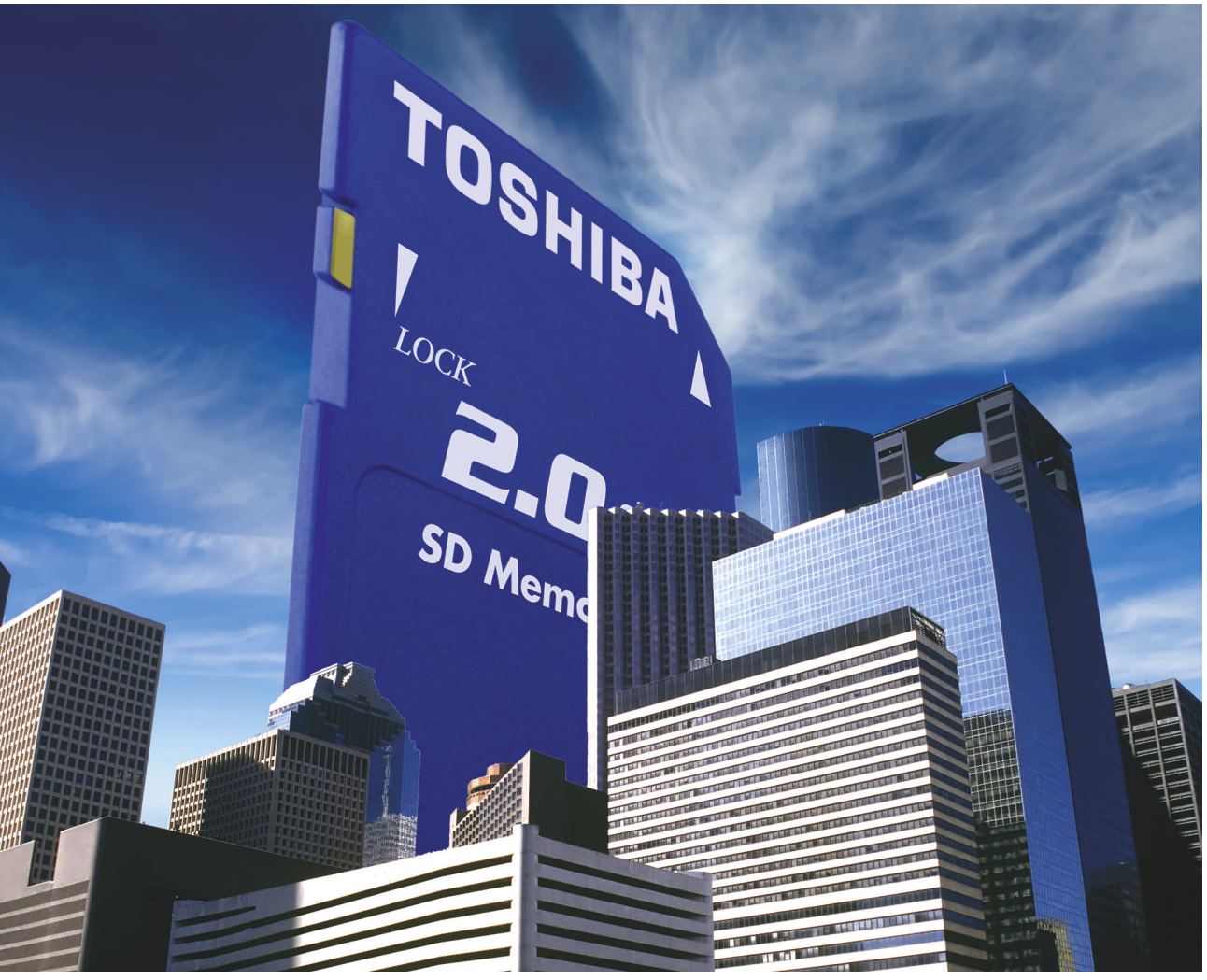

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An overview of on-chip compression architectures

DATA-COMPRESSION TECHNIQUES CAN HELP MANAGE THE ESCALATING COST OF TEST IN NANOMETER DESIGNS.

The test time that scan tests require typically dominates manufacturing-test costs for digital designs. The increase in design complexity and the requirements for delay tests have made test time a design parameter that requires active management in nanometer designs. As the number of patterns increases, it takes more tester-buffer space to hold the complete test set, and it takes longer to execute the test set in manufacturing. To address both the data-volume and test-time problems, test engineers and test architects have developed techniques employing on-chip hardware that compresses the test-stimulus and response patterns and then applies them to the chip under test. Luckily, there are many test architectures that engineers can employ for test-data compression.

COMPRESSION-METHODS BACKGROUND

The dominant method of testing digital circuits is the use of an ATPG (automatic test-pattern generator) to target a stuck-at or transition fault model at all of the circuit nodes. In circuits that contain storage elements, engineers can use scan registers to enable control and observation of the storage elements and ensure high fault coverage. When the ATPG generates too many test patterns, the test-application time becomes too long, and engineers must use on-chip-compression techniques to minimize test time and, thus, test costs.

Test compression builds on technology originally developed for LBIST (logic built-in self-test). **Figure 1** shows the general structure of compression logic within a chip or core. The system decompresses a compressed input stream and feeds it into the internal scan chains, some of which may be inside cores within the design. The system optionally feeds the output from the internal scan chains through masking logic and then compresses it into an output stream. Engineers can use several architectures for the input decompressor and the output compressor.

INPUT DECOMPRESSION

Input decompression enables a small number of scan input streams to load stimulus into a much larger set of internal scan chains. Papers have proposed and products have implemented several types of input-decompression architectures. **Table 1** lists the most common.

The simplest input decompressor is broadcast scan. This device simply fans out each scan input to multiple internal chains. The main complaint against broadcast scan is that those chains receiving their values from the same scan-in pin have directly correlated values, which may impact fault coverage. In most practical implementations, however, this possibility has not been a problem. Engineers obtain the linear-spreader, space-expansion network by XORing combinations of scan inputs to each internal-chain input. The scan correlations are still there, but they are less direct than with broadcast scan.

Another approach to avoiding the scan-chain dependency associated with broadcast scan is the use of multiplexed scan configurations. In its simplest form, this technique uses several broadcast-scan configurations and provides one or more additional scan inputs to switch between them. The scan correlations are still there, but, for some scan cycles, one of the configurations may allow you to attain the desired care bits. A multiplexed linear spreader is similar to the multiplexed broadcast scan. It provides two or more sets of linear equations that you can use to solve and attain the desired care bits from the ATPG.

Alternative approaches for input decompression rely on a sequential linear-feedback and spreading network. The sequential elements are based on LFSRs (linear-feedback-shift registers) or linear automata, but they achieve the same result: Buffer up the input variables from the scan-input streams so that scan cycles not requiring a lot of care bits can defer the use of the variables for later, more demanding cycles. These approaches are almost assuredly the best for dealing with any scan correlation. However, the scan chains still see correlated values, so

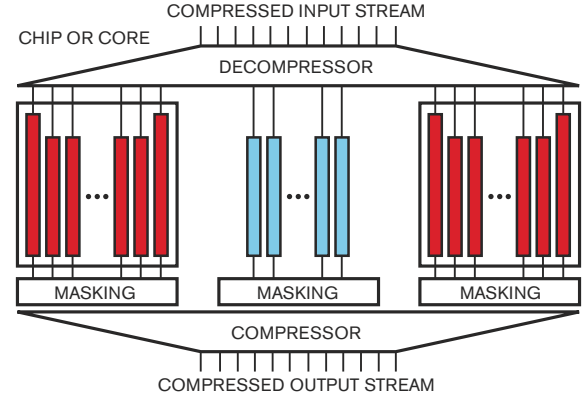

Figure 1 In a general-compression structure, engineers decompress a compressed input stream and feed it into the internal scan chains, some of which may be inside cores within the design.

there are limits to how many care bits one scan cycle or consecutive scan cycles can accommodate.

OUTPUT COMPRESSION

The role of an output compressor is to enable a large number of internal scan-chain output streams to merge to create either a much smaller set of external scan-output streams or to create a signature for each test or set of tests. **Table 2** lists the most common compressors, many of which papers have proposed and products have implemented.

The simplest compressor, an XOR tree, computes simple parity of its inputs. This method has two major limitations: aliasing and X tolerance. If engineers feed each internal-chain output to one scan-output pin through a parity tree and if an equal number of inputs to the parity tree contain errors, the error will be lost due to cancellation. Unknown values (X states) in any chain output mask any other chain feeding the same scan output. Diagnostics of tester failures are possible by assuming that any error bit in the output stream could have come from any of the internal chains that feed to that output. Although this technique causes the simulation of many more faults than would be necessary without compression, it likely reduces diagnostic accuracy over uncompressed analysis.

One method of reducing the limitations of the XOR-tree space compactor is to combine it with input fan-out to help deal with both the aliasing problem and the issue of unknown (X) values. Here, each internal chain feeds to a unique set of scan outputs, with each scan output fed by an XOR tree of values from some set of chain outputs. Defining a space compactor that can deal with a large number of X values in the same scan cycle requires a large amount of fan-out, making it prohibitively expensive to implement. The more fan-out, the likelier that a larger number of X values in the same cycle will cause every output to be X. Unless you know that there will not be a large number of X values in any scan cycle, this approach will likely require some amount of X-masking capability. Diagnostics become more difficult, because errors now tend to appear on multiple output pins; simply picking all internal chains that feed any of the failing outputs produces too many candidates. Solving simultaneous equations to locate the most likely source or sources of the errors can help to reduce the number of candidates to consider for capturing the defect's effect and thus reduce the number of faults to simulate.

The multiplexed-output-select approach consists of a multiplexed internal-chain-output-select network using inputs to select which set of chain outputs each scan cycle should observe. This approach often causes the system to ignore most of the chain outputs and thus may miss some of the accidental detections that occur. It is unclear how detrimental this approach might be, but few defects in today's technologies behave exactly like the faults in the ATPG-fault model. Selecting the chain outputs to observe takes care of much of the necessary masking to avoid X values. As long as there is no combining of values from multiple internal chain outputs, there should be neither a need to add X-masking to such a compressor nor an issue with aliasing. Diagnostics are much simpler for this approach, because there is only one source of the error when it is seen at a scan output—the internal chain selected on that scan cycle. However, because the system does not observe many of the additional errors that typically occur when devices fail, it may be difficult for diagnostic-fault simulation to correctly assess the location of the failure with such a reduced response set.

Convolutional compactors add a linear shift register to the output-space-compactor network. Its advantage is that it reduces the aliasing problem associated with a simple XOR tree. The addition of the shift register also may reduce the ability of the compactor to deal with unknown values (X). An X value corrupts the bits in the register and anything they feed, but the X eventually drops out of the register. Diagnostics are more complicated and, again, likely to require the simulation of many more faults than if no compression took place.

Finally, for decades, engineers have used MISRs (multiple input-shift registers) to compress responses, and MISRs are necessary for any form of BIST. The output data continually clocks into the MISR, and, at the end of the test, the signature in the MISR assesses a pass or fail versus the known-good signature. MISRs have some small chance for aliasing in which the defect produces a signature that matches the defect-free circuit, but the likelihood is normally much smaller than the missed faults due to poor fault coverage. The biggest benefit of using a MISR is that response data compression is highest with a MISR, because there is no need to compare output values on every scan cycle—only the final state. It is even possible to collect a signature across all of the tests and check it only at the end of the test set. MISRs cannot tolerate any X values. Using a MISR requires the use of X-masking to prevent any X values from getting into the MISR unless all X sources have been

TABLE 1 COMMON INPUT DECOMPRESSORS

Input decompressor	Comment
Broadcast scan	The simplest input-decompression scheme
Linear (XOR) spreader	A combinatorial input decompression, requires linear-equation solver
Multiplexed broadcast scan	Alleviates scan correlation from broadcast scan by switching between several broadcast-scan configurations
Multiplexed linear spreader	Alleviates scan correlation from linear spreader by switching between several spreader configurations, requires linear-equation solver
Linear-automata stream	Alleviates scan correlation from linear spreader by circulating input variables within FSM, requires sequential linear-equation solver

TABLE 2 COMMON OUTPUT COMPRESSORS

Output compressor	Combinatorial/ sequential	Comment
Space compactor (XOR tree) using only fan-in	Combinatorial	Could alias (lose) errors from even number of chains or when combined with unknown (X) values
Space compactor with fan-out	Combinatorial	Less chance of aliasing, can handle some X
Multiplexed output selects	Combinatorial	May miss accidental detects, can handle X
Convolutional compactor	Sequential	Less chance of aliasing, can handle some X
MISR with space compactor	Sequential	Less chance of aliasing, cannot handle X

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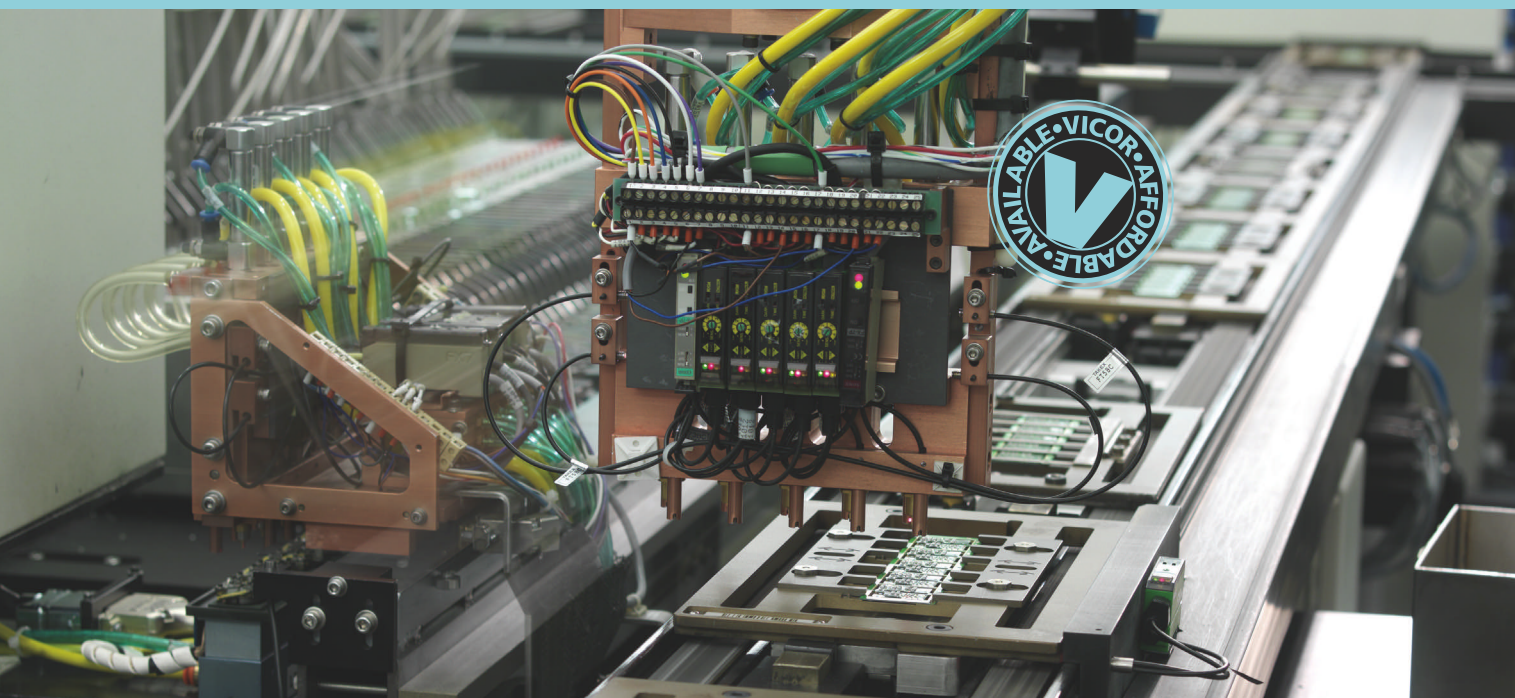

blocked. Also, diagnosing failures from the final MISR signatures is highly unlikely. Knowing which of several MISRs caught the error may help isolate the error to a single core or area of the chip but not to a specific failing net. Diagnostics with MISRs typically require either reapplying the test and scan-out (without compression) to collect the diagnostic fail data or to observe the state of the MISR on each shift cycle to catch where the errors enter the MISR on each cycle. One alternative is to add a few uncompressed vectors to the compressed test set and perform diagnostics primarily for failures that occur within that smaller, uncompressed test set.

DEALING WITH UNKNOWN VALUES

A typical design with tests generated by an ATPG has unknown logic values that propagate in the scan chains to the output streams. Except for the multiplexed-output selects, compression logic loses efficiency when it has to contend with a large number of unknown or unpredictable values in the output streams. This situation is a concern for any compression scheme that relies on MISRs to compute signatures, but it also can cause non-MISR-based results to suffer. All compression schemes except the multiplexed-output approach linearly merge the output streams and thus are affected when an X merges with non-X values, causing the ATPG to ignore and effectively mask out some of the non-X internal-response values. As more unknown values become part of the output stream, engineers may have a tough time seeing defective responses, possibly resulting in a loss of fault coverage or an increase in test-vector count to make up for the fact that such tests detect fewer faults, either those that the ATPG targets or those that emerge by accident.

One way to alleviate the problem of unpredictable values in the output stream is to mask these values before they enter the compressor. In the case of MISRs, this step may be necessary to avoid the creation of corrupted and unpredictable MISR signatures. In the case of the space-compactor approaches, it may be necessary just to allow detection of certain faults; there is no absolute requirement to mask out all X values. However, because X values that do propagate through mask out known values from some chains when too many X values do appear on the same scan cycle, only a few chains may be observable on that cycle. This situation reduces the ability to see where additional errors may have been and reduces the ability of diagnostics to locate the true failure location.

Masking out some values while allowing others to pass requires you to pass some information into the device. Thus, adding an X-masking capability consumes more of the input bandwidth, possibly taking that bandwidth away from care bits that target faults. Remember, however, that the observation points for faults are also effectively care bits in this compression environment. So, it is not unreasonable to allocate some of the input-side bandwidth to the X-masking.

INTEROPERABILITY REQUIREMENTS

Typically, vendors insert compression architectures at the RTL or gate level, and the ATPG and diagnostics engines need to understand the architecture of the compression to generate

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DESIGN NOTES

High Resolution Video Solutions Using Single 5V Power

Design Note 396

Jon Munson

Introduction

Video cable driver amplifier output stages traditionally require a supply voltage of at least 6V in order to provide the required output swing. This requirement is usually met with 5V supplies by adding a boost regulator or a small local negative rail, say via the popular LT®1983-3. Such additional circuitry is unnecessary in typical $1V_{P-P}$ video connections, such as HD component video, if the cable driver amplifiers simply offer near rail-to-rail output capability when powered from 5V.

Standard definition and SVGA (800×600 pixel) low voltage devices have been available from Linear Technology for some time (see Design Note 327), but a number of recent device developments have made it possible to produce high resolution video devices that operate on a single 5V power supply. Some parts that fit this mold include the LT6556, a UXGA-resolution (1600 × 1200 pixel) RGB 2:1 input-port buffered multiplexer (MUX); the LT6557 and LT6558 UXGA fixed gain triple amplifiers that include on-chip biasing to minimize external part count; and the LT6559 triple amplifier that provides flexible, cost effective solutions in SXGA (1280 × 1024 pixel) products.

High Resolution Video Input-Port Multiplexer

High performance multimedia video display systems usually include a multiple-input feature to select between a VESA-compliant D-type PC connection and consumer component video that uses RCA jacks. The incoming video signal is at most $1V_{P-P}$ nominal (Y-channel,

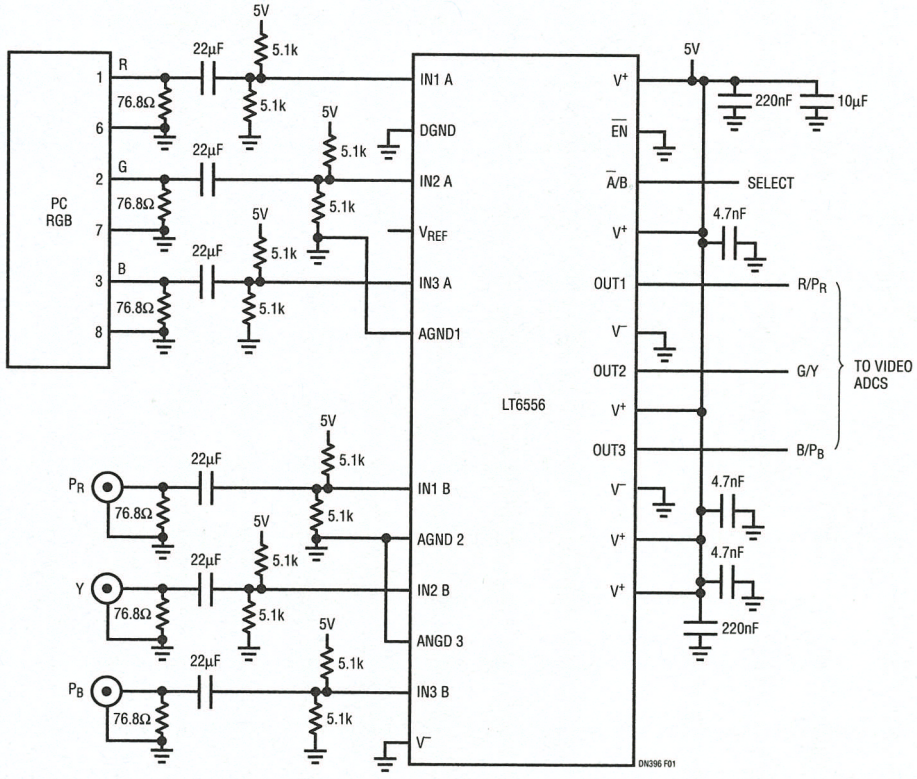

Figure 1. LT6556 Provides Input Video Selector and ADC Driver for Multimedia Display System

1.5V_{P-P} worst-case when AC-coupled) and the required gain is unity for digitizing by an analog-to-digital converter set (ADC) or other signal routing. This input selection function is readily implemented with the LT6556 on 5V as shown in Figure 1, supporting all video resolutions including UXGA by virtue of its 750MHz bandwidth and 6.5ns settling time. The part is available in either SSOP-24 or QFN-24 packaging and includes layout-friendly flow through pinouts. For the AC-coupling shown, the outputs swing approximately ±0.7V about the mid-supply level, within an available range of 2.6V_{P-P}. Though not explicitly shown in Figure 1, coupling to the ADC inputs usually involves series resistances to reduce capacitive loading of the amplifiers to preserve the smoothest frequency response and optimal settling.

High Resolution Single-Supply Cable Driver

The LT6557 is a triple video amplifier specifically engineered to provide UXGA level performance on a single 5V power supply. A quasi rail-to-rail output stage and an almost slew-unlimited 400MHz large signal bandwidth make this the part of choice for the most performance-critical applications.

The LT6557 has internal gain-setting resistors to establish a nominal gain of two and incorporates a single-resistor-programmable input biasing system to eliminate the usual input divider resistors used in single supply applications. As seen in Figure 2, the entire cable driver function is largely reduced to the IC and blocking capacitors. The internal input biasing may be defeated for DC-coupled applications, such as with direct digital-to-analog converter (DAC) output applications where a software controlled offset is introduced to set the signal dynamics. A unity gain version, the LT6558, is also available.

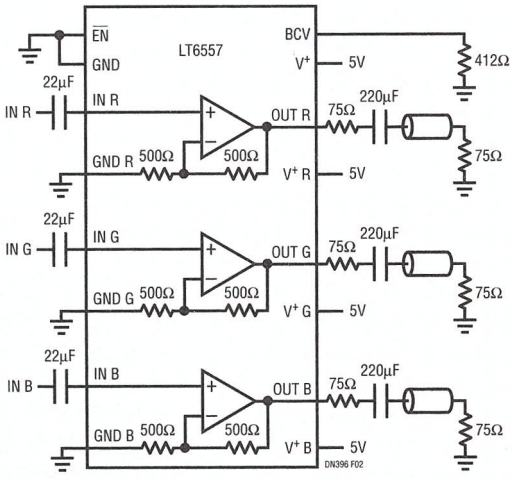

Figure 2. LT6557 Provides Low Part Count UXGA-Resolution Cable Driver on 5V Supply

Economical SXGA/HD Cable Driver

In cost sensitive applications like consumer video-playback equipment, the LT6559 provides excellent bang-for-the-buck in a tiny QFN-16 (3mm × 3mm) package. As a basic triple current-feedback op amp (CFA) with individual channel enables, the LT6559 offers great flexibility in forming various multiplexer, cable driver, and ADC driver functions at low cost. Even though the LT6559 is not a true rail-to-rail output device, there remains approximately 3V_{P-P} of available output swing on 5V due to its high performance output stage design. Figure 3 shows a typical AC-coupled application as an economical HD or SXGA-grade triple cable driver (one channel shown for brevity). As a general purpose CFA, the feedback resistor value (301Ω) optimizes the frequency response. This circuit is ideal as an output buffer/driver for following passive reconstruction filters such as for the increasingly popular 1080p HD format (i.e. 60MHz lowpass).

Conclusion

As system designers continue to reduce the number of supply voltages used within their products, pressure to maximize analog performance on available 5V logic supplies has led to the need for viable low voltage high performance video solutions. For high resolution applications, Linear Technology offers the LT6556 buffered MUX, the LT6557/LT6558 AC-coupled amps, and the economical LT6559 triple CFA—all well suited to operate in the 5V environment.

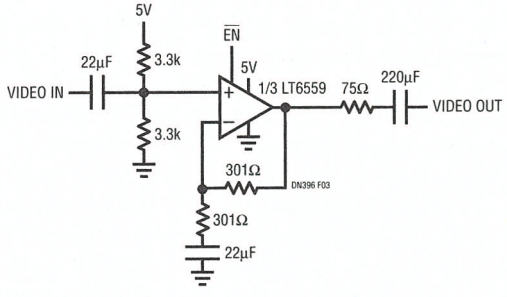

Figure 3. HD Video Cable Driver Using Economical LT6559 (Depicting One Channel of Three)

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and diagnose tests with these structures on-chip. The supplier that inserts the compression then also by default becomes the ATPG and diagnostics supplier. Semiconductor companies, however, often demand choices for ATPG and diagnostics from multiple vendors for a given application. As a result, the industry is moving toward enabling interoperability of ATPG and diagnostics for different compression architectures. The Accellera Consortium (www.accellera.org) of EDA vendors and users launched an OCI (Open Compression Interface) technical committee within the last year. The OCI technical committee is defining a standard that you can use to describe the required information about on-chip compression structures to ATPG and diagnostics tools. More information is available at the Accellera Web site (**Reference 1**).

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Test-data-compression techniques manage the escalating cost of test in nanometer designs. As designers adopt delay test to detect small delay defects in nanometer designs, they will also adopt on-chip compression methods. Luckily, the test industry has developed several popular compression structures over the past few years and will continue development as new challenges arise. EDN

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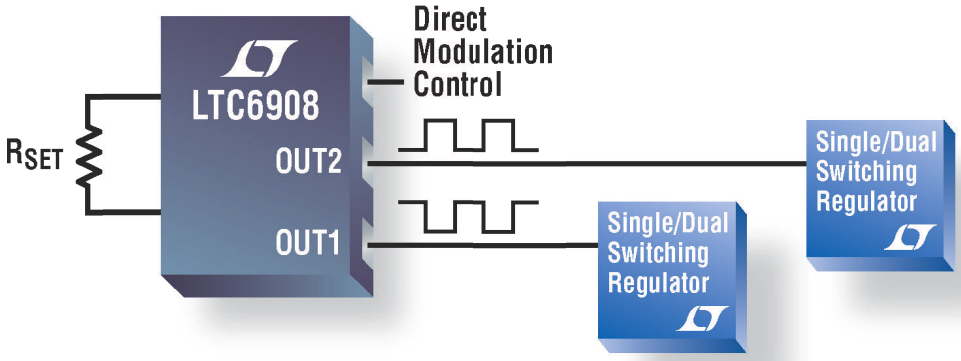
AUTHOR'S BIOGRAPHY

Brion Keller is a senior architect at Cadence Design Systems. He has 27 years of experience in ATPG, fault modeling and simulation, logic BIST, test-vector compression, diagnostics, and general design for test, including more than 23 years at IBM. Keller has a bachelor's degree in computer science and chemical engineering from Pennsylvania State University (University Park).

Tiny Clock Optimized for Switchers



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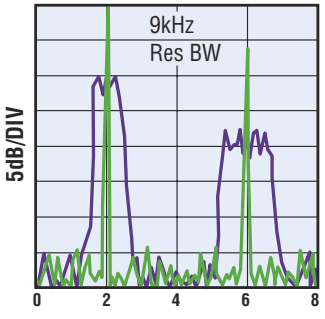

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LTC3210/-1	2.9 to 4.5	500	2	Main, CAM	5	1-wire	3 x 3 QFN-16
LTC3217	2.9 to 4.5	600	1	CAM	4**	Resistor/PWM	3 x 3 QFN-16
LTC3214	2.9 to 4.5	500	1	CAM	1**	Resistor/PWM	3 x 3 DFN-10
LTC3216	2.9 to 4.4	1000	1	CAM	1**	Resistor/PWM	3 x 4 DFN-12

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designideas

READERS SOLVE DESIGN PROBLEMS

PIC microprocessor drives 20-LED dot- or bar-graph display

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

The circuit in **Figure 1** uses only five I/O lines to drive a dot- or bar-graph display of 20 LEDs. Although this version of the design uses a small and inexpensive one-time-programmable microprocessor, such as a Microchip (www.microchip.com) PIC12C508A, you can use other microprocessors with N I/O lines to drive as many as $N\times(N-1)$ LEDs. For software development or modification, you can use a PIC12C508A-JW reprogrammable-EPROM version of the PIC12C508A, or you can substitute a less expensive PIC16F84A with flash memory.

To avoid application of excessive reverse voltage to the LEDs, the circuit's power supply, V_{DD}, must not exceed 3V dc. You can drive other types of loads and provide electrically isolated interfaces by replacing the LEDs with appropriately rated optocouplers. For demonstration purposes, IC_1's input line, GP3, connects to a pushbutton display-mode-selector switch and a pulldown resistor that simulates a digital-input-signal source with a voltage amplitude of 3V p-p.

Listing 1, available with the online version of this Design Idea at www.edn.com/060901di1, performs a variety of functions. To conserve battery power, the basic software drives one LED at a time in dot or bar mode with a minimum amount of current. Approximately 2 mA flashes a high-brightness LED. The software includes a delay routine that solves the problem of contact bounce. Tests show that a miniature pushbutton switch requires a delay of at least 1 msec for successful debouncing.

Consuming fewer than 256 words, the software avoids a C12C508A programming restriction that requires placement of subroutines only in page 0. Other features of the software include a two-level stack, the use of files common to both the PIC12C508A and

DIs Inside

72 PC's serial port controls programmable sine-wave generator

74 I²C interface connects CompactFlash card to microcontroller

76 IC and DMM form direct-readout temperature probe

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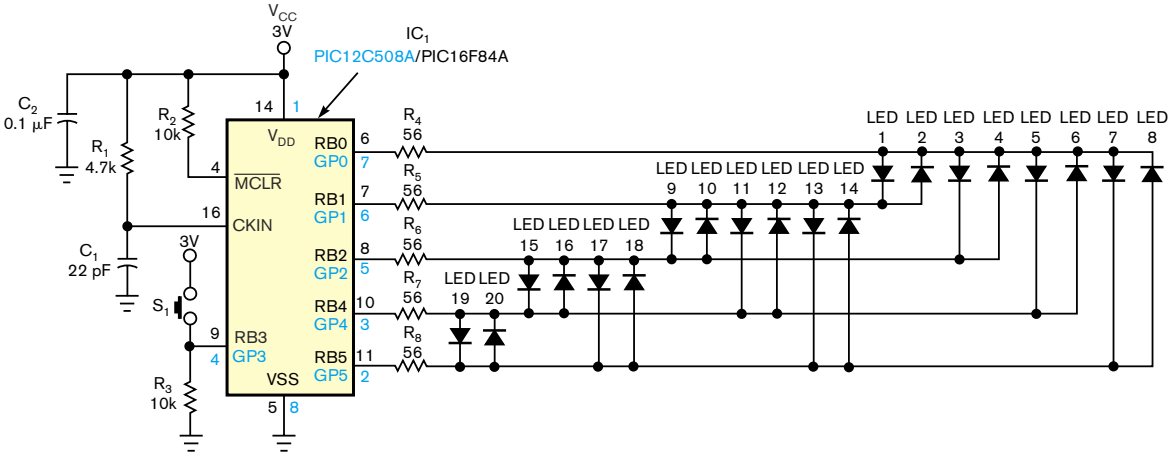


Figure 1 A dot- or bar-graph display uses either a one-time-programmable PIC12C508A or, for experimentation, a reprogrammable and reusable PIC16F84A. Use high-brightness diodes for LED 1 through LED 20.

the PIC16F84A in the $0C_H$ to $1F_H$ range, use of the RETLW 00_H instruction instead of Return, and avoidance of the ADDLW and SUBLW instructions. The software defaults to the dot-display mode. Pressing and holding S_1 before and during power application selects the bar-display mode. Note that the configuration settings for the MPASM assembler vary according to which microprocessor you select for programming. EDN

PC's serial port controls programmable sine-wave generator

Yongping Xia, Navcom Technology, Torrance, CA

This Design Idea describes a circuit that uses a PC's serial port to control a sine-wave generator that covers a frequency range of 2 Hz to 20 kHz in 1-Hz steps (**Figure 1**). The circuit's output voltage of approximately 2.2V p-p remains constant over the entire frequency range. The circuit's signal source, a Linear Technology (www.linear.com) LTC6904, IC_1, consists of a digitally programmable square-wave oscillator that, without using a clock crystal, covers a frequency of approximately 1 kHz to 68 MHz at 0.1% resolution and a few percentage points of accuracy. The LTC6904 features an I^2C serial-communications interface that controls the output frequency according to: $OSC_{CLK}=2a\times 2078\ Hz/[2-(b/1024)]$. The variables "a" and "b" represent 4- and 10-bit digital codes, respectively, and the equation's frequency unit, OSC_{CLK}, is in hertz.

The OSC_{CLK} output from IC_1 at Pin 6 drives IC_2, a 14-stage 74HC4020 binary counter whose outputs at Q4 and Q10 serve as the clock and input signals for IC_3, a Maxim (www.maxim-ic.com) eighth-order, switched-capacitor MAX291 lowpass filter.

The −3-dB corner of the filter's frequency response occurs at one-one-hundredth of IC_3's clock frequency. Fixed at one-sixty-fourth of the clock-signal frequency, only the input square wave's fundamental frequency can pass the filter without undergoing considerable attenuation. The filter's eighth-order response removes higher order harmonics, and the filter's output thus consists of a sine wave at the input's fundamental frequency. The filter's clock and input always occur in a 64-to-1 frequency ratio, and the sine wave's output amplitude thus remains constant over the entire frequency range.

To generate a 1-kHz sine wave, the circuit requires a filter clock at a frequency of 64 kHz, which sets the OSC_{CLK} frequency 64 times higher, or 1.024 MHz. To satisfy the equation, the LTC6904 requires programming constants of $a=09_H$ and $b=3d8_H$ to generate an OSC_{CLK} frequency of 1023.94 kHz and the nearest output frequency of 999.9 Hz.

Written for IBM-compatible PCs, the C-language program accompanying this Design Idea, which is available at www.edn.com/060901di2, accepts an

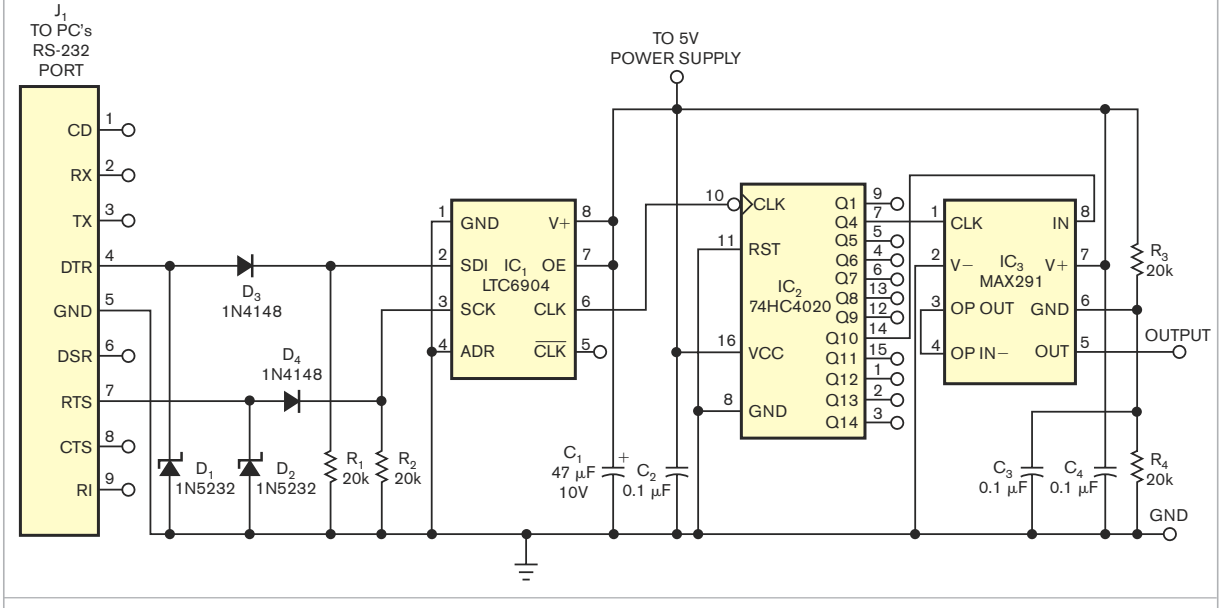
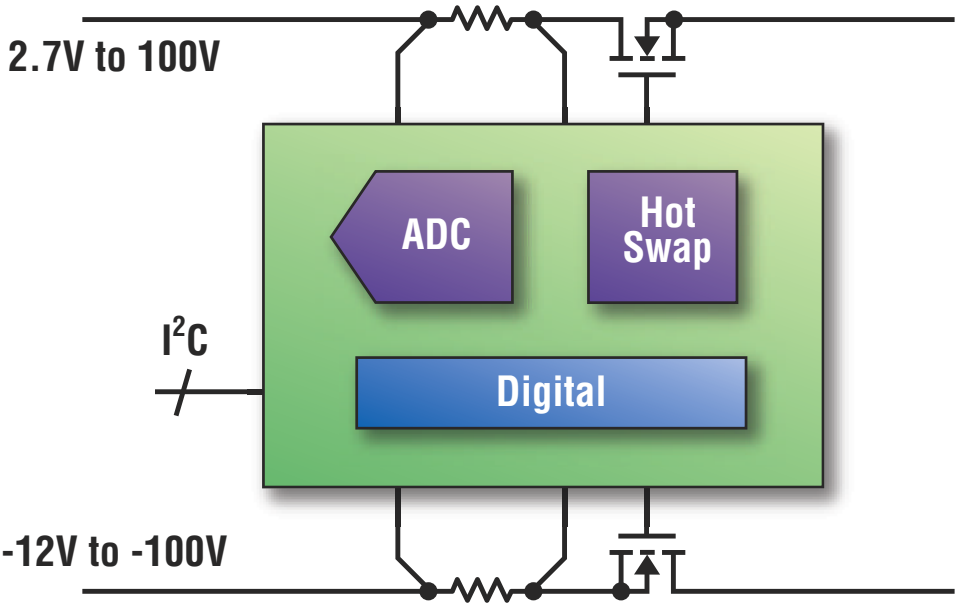


Figure 1 Three ICs and a few passive components generate sine waves under the control of a PC's serial port.

Digital Hot Swap



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output-frequency request, calculates the nearest values of programming codes "a" and "b," transmits the codes to IC_1, and shows the calculated frequency on the PC's display. Although a PC's serial port delivers RS-232 signals, diodes D_1 through D_4 limit the voltages available at Pin 4, the data-terminal-ready pin, and Pin 7, the ready-to-send pin, to levels compatible with the I²C bus's SDI and SCK signals, respectively. EDN

I²C interface connects CompactFlash card to microcontroller

Fons Janssen, Maxim Integrated Products Inc, Sunnyvale, CA

Logging data from a large number of monitored channels usually requires a lot of memory for storing the measured data. Unfortunately, smaller microcontrollers offer only limited amounts of internal data RAM and EEPROM and may also lack spare address and data ports for adding external memory. Many low-end microcontrollers include an industry-standard I²C interface for attaching external ADCs, DACs, real-time clocks, and other peripherals.

The circuit in **Figure 1** connects a CompactFlash card to a microcontroller's I²C interface through IC_1, a 16-bit I²C I/O extender. In memory-mapped mode, an 8-bit-wide data bus controls the CompactFlash card. Microcontroller IC_1's Port 1 (I/O lines 0 through 7) connects to the CompactFlash card's data bus and provides read and write access to the card's data registers. Port 2 provides the card's address and control registers and generates the read and write signals.

To write to a register, configure Port 1 as an output and write the data to the port. Next, write the register-control data three consecutive times to Port 2 while toggling the port's WR_N pin from Logic 1 to Logic 0 to Logic 1 to generate the "write" signal. Address bits A2, A1, and A0 select the register that receives the written data. Applying Logic 0 to the CE pin while RD_N rests at Logic 1 enables the CompactFlash card. To read from a register, configure Port 1 as an input port and apply three writes to Port 2 while toggling the port's RD_N pin from Logic 1 to Logic 0 to Logic 1 to generate the "read" signal.

After the three writes, the microcontroller reads Port 1 and makes the data available. Address bits A2, A1, and A0 address eight internal registers and allow read and write access (**Table 1**). Register 0x00 contains data for exchange between the host and the CompactFlash card. Registers 0x03, 0x04, 0x05, and 0x06 specify the track

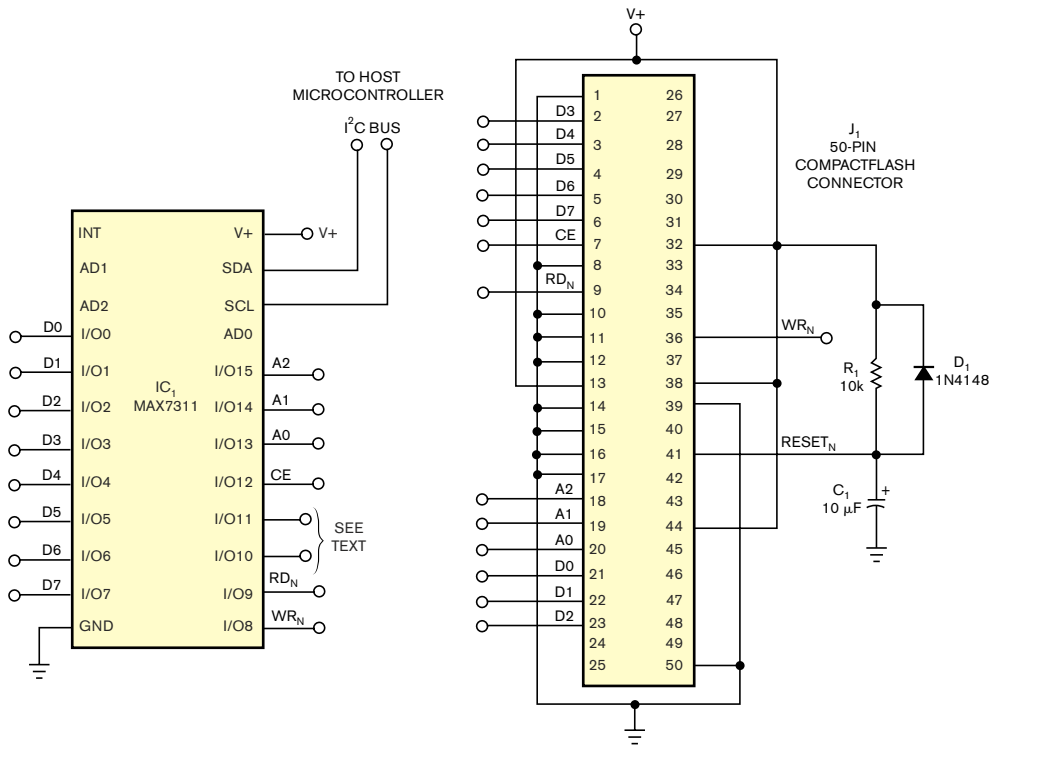

Figure 1 A 16-bit I/O extender, IC_1, and a CompactFlash connector add external data storage to a microcontroller's I²C bus.

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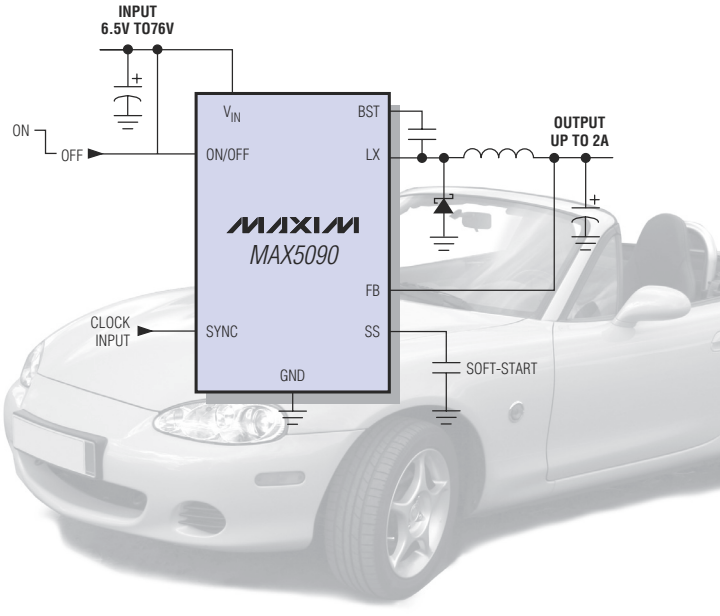

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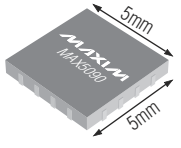

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for reading or writing data. Each track contains 512 data bytes. The processor indicates reading and writing tracks and other functions by writing to 0x07, the command register, and registers 0x01 and 0x07 contain error conditions and status information.

Two unused pins, 10 and 11, on Port 2 are available to drive LEDs that display circuit activity and status. As an alternative, the pins can support a user-installed configuration jumper. In this configuration, IC_1's interrupt output should connect to the host microcontroller's interrupt input so that installation or removal of the jumper can signal the microcontroller to recognize or ignore the CompactFlash card. Selecting a CompactFlash-card connector with hot-plugging contacts allows insertion or removal of a card without switching off power or disturbing an ongoing data-logging process.

With software modifications, a host microcontroller can switch between two CompactFlash cards. Adding a second MAX7311 supports an additional CompactFlash card and expands the circuit's storage capacity, and the hot-plug feature supports removal of a fully loaded card for data processing on another system. Microcontrollers that include hardware-based I^2C interfaces can use two relatively simple I^2C software functions to read and write a CompactFlash card through IC_1's I/O ports.

The first function is: Write_MAX 3711(slv,prt,dat). This procedure starts the I^2C bus and sends a data byte (dat) to a port (prt) on the MAX7311 using a slave address (slv). The other procedure, Read_MAX3711(slv,prt), starts the I^2C bus and reads a data byte from a port on the MAX7311 at a slave address. These functions serve as foundations for two additional functions, which read and write to the CompactFlash card's registers. The first, Write_CF_REG(reg,dat), uses Write_MAX3711 to place the data on Port 1. Use the same procedure to place the register address (reg) and other control signals on Port 2. Executing this function three times while toggling WR_N generates the write signal. The Read_CF_REG(reg) procedure uses Write_MAX7311 to address the CompactFlash card's register and generates the read signal. Invoking Read_MAX 7311 then reads the data from the register.

These functions, which in turn read and write the card's registers, create functions that access the CompactFlash-card sectors: Write_CF(cyl, head,sec). To perform a write operation, this procedure uses Write_CF_REG to designate the CompactFlash card's target cylinder, head, and sector registers (0x03 to 0x06). Next, writing 0x30 to the command register configures the CompactFlash card to accept data. Executing Write_CF_REG 512 times writes data in the microcontroller's global array to the data register. The CompactFlash card automatically adds this data to the current track. To perform a read operation, the Read_CF(cyl,head,sec) procedure uses Write_CF_REG to designate the target cylinder, head, and sector. Next, writing 0x20 to the command register configures the CompactFlash card to deliver data to the host processor. Executing Read_CF_REG 512 times reads all 512 bytes through the data register from the current CompactFlash card's track and places the data in a global array.

If the microcontroller lacks sufficient internal memory to store 512 data bytes, the software can write each digitized data-point measurement directly to the CompactFlash card. For additional information on controlling CompactFlash cards, review the material in **Reference 1**. EDN

TABLE 1 ADDRESSES AND REGISTERS

Address	Register	Address	Register
0x00	Data	0x04	Cylinder low
0x01	Error/features	0x05	Cylinder high
0x02	Sector count	0x06	Select card/head
0x03	Sector number	0x07	Status/command

REFERENCE

1. CF+ and CompactFlash specification, www.compactflash.org.

IC and DMM form direct-read-out temperature probe

Alfredo H Saab and Bich Pham,
Maxim Integrated Products Inc, Sunnyvale CA

The simple temperature-measurement probe in **Figure 1** can serve as an indispensable tool for troubleshooting and debugging electronic circuits. To measure temperature at several points, you can equip IC_1, a Maxim (www.maxim-ic.com) MAX-6610, with a probe, or you can permanently integrate one or more devices into a pc board or attach them to components. Resistors R_1, R_2, and R_3 set the circuit's temperature-scaled voltage output to various values (**Table 1**). **Figure 2** shows the circuit's representative output versus temperature.

You can display the circuit's temperature-proportional dc output voltage on any DVM (digital voltmeter) or handheld DMM (digital multimeter). The circuit draws only 200 µA from a nominal 3V power supply, such as a pair of AA alkaline cells. A CR2016 lithium-coin cell can operate the circuit continuously for several hundred hours or for several years if you equip the circuit with a normally open, momentary-contact pushbutton switch.

To produce the error curve in **Figure 3**, immerse the circuit and a platinum-resistance standard thermometer in a

TINY I/O EXPANDERS HAVE 240-STEP PWM BRIGHTNESS CONTROL FOR RGB LEDs

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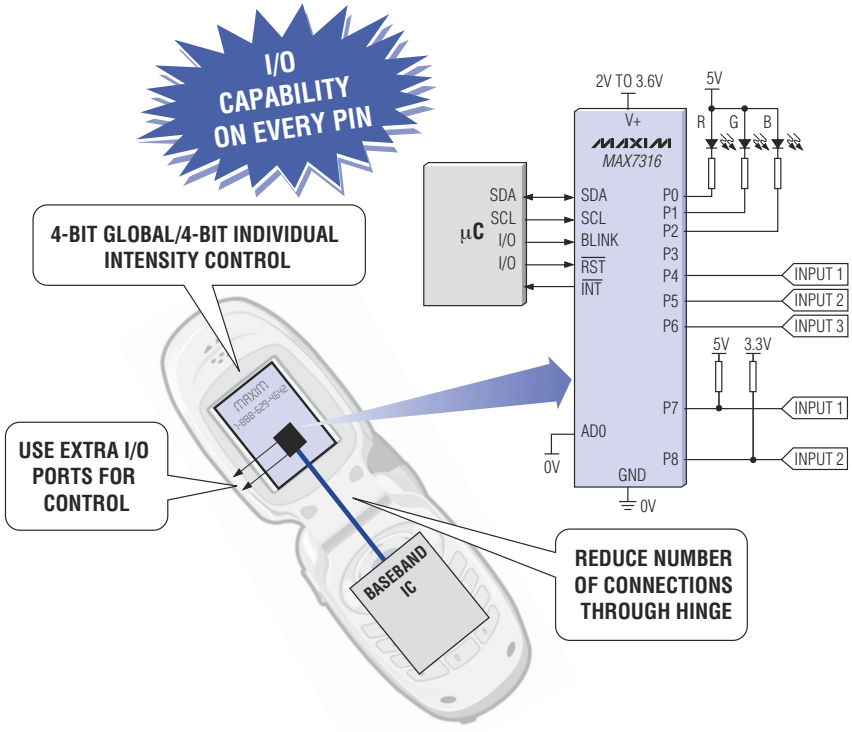

- ♦ Low 1µA (typ) Standby Current
- ♦ All Ports Can Sink 50mA Continuous Current
- ♦ Available in Space-Saving Packages
  - ♦ TQFN
    - 3mm x 3mm (16-Pin)
    - 4mm x 4mm (24-Pin)
  - ♦ QSOP
  - ♦ TSSOP

The MAX7313–MAX7316/MAX6964/MAX6965 drive from 8 to 18 LEDs. They feature an integrated 240-step PWM brightness control to drive RGB LEDs or white LED backlights with global and individual dimming control. LED blink control is standard, and I/O reset is available on select devices. The MAX7313–MAX7316 have I/O capability on each port and interrupt output upon transition detect (optional on some devices). The MAX6964 and MAX6965 are optimized for LEDs with output only, 7V-tolerant ports. Available in tiny TQFN packages and with low standby current (1.2µA, typ), these parts are ideal for portable or space-constrained applications.

Part	No. of Ports	I/O Port Tolerance (V)	Interrupt	Reset	Blink	Pin-Package
MAX7313	16	5	Yes	—	—	24-TQFN, 24-QSOP
MAX7314	18	5	Yes	Yes	Yes	24-TQFN, 24-QSOP
MAX7315	8	5	Yes	—	—	16-TQFN, 16-QSOP, 16-TSSOP
MAX7316	10	5	Yes	Yes	Yes	16-TQFN, 16-QSOP, 16-TSSOP
MAX6964	17/GPO	7	—	Yes	Yes	24-TQFN, 24-QSOP
MAX6965	9/GPO	7	—	Yes	Yes	16-TQFN, 16-QSOP, 16-TSSOP

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temperature-controlled oil bath. The circuit's relative error with respect to the standard thermometer varies only 4°C over −40 to +125°C. The MAX6610's data sheet includes additional information on temperature-measurement error and output range.

To apply the circuit as a temperature probe, solder a 5-mm length of 1-mm-diameter, uninsulated copper wire directly to a small copper pad at IC_1's GND pin. The wire should make thermal and electrical contact with the GND pin and thus provide a path of low thermal resistance from the sensor IC to the point of probing. Glue the wire to the pc board to add mechanical support. Heat loss affects the temperature measurement's accuracy, and, to minimize heat loss from the probe through the pc board, use long and thin copper traces to make electrical connections from IC_1 to its supporting components.

Applying the MAX6610 as a pc-board temperature sensor differs somewhat from using it as a temperature probe. For board-temperature sensing, IC_1 must reside in intimate thermal contact with the board. Connect large copper areas immediately to the IC's pins and use short, thick traces—or none at all—between the copper areas and the IC's pins. The copper areas guarantee accurate temperature readings by providing thermal contact with the board and good heat transfer between the board and the sensor. EDN

REFERENCE

1 "Precision, Low-Power, 6-pin SOT23 Temperature Sensors and Voltage References," MAX6610/6611 data sheet, Maxim Integrated Products, November 2003, http://pdfserv.maxim-ic.com/en/ds/MAX6610-MAX6611.pdf.

TABLE 1 TEMPERATURE-SCALED VOLTAGE OUTPUT

	10 mV/°C	1 mV/°C	1 mV/°F
R_1 (kΩ)	68.1	68.1	68.1
R_2 (kΩ)	2.8	2.8	19.6
R_3 (kΩ)	Open	2.21	3.32

Note: All resistors are of ±10% tolerance.

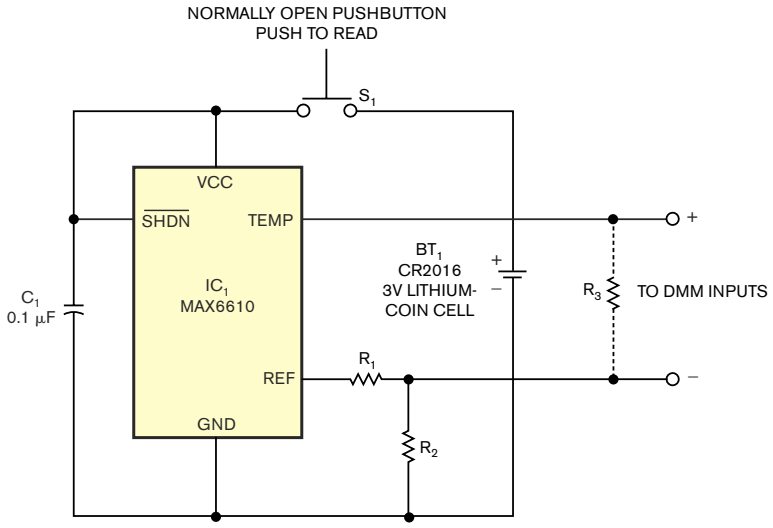

Figure 1 One IC and a few passive parts directly display temperature on an external voltmeter. See Table 1 for values for R_1, R_2, and R_3.

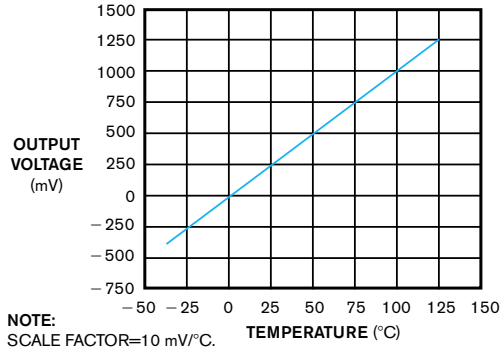

Figure 2 The circuit of Figure 1 exhibits a nearly linear output-voltage-versus-temperature characteristic.

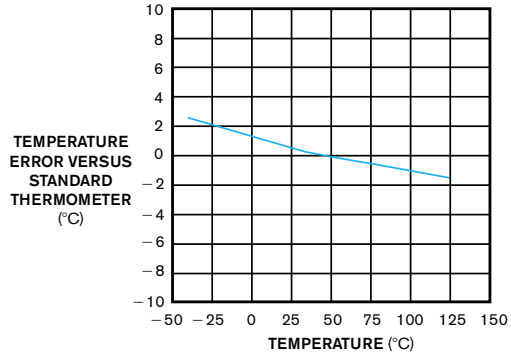

Figure 3 Immersed in a temperature-controlled oil bath and compared with a platinum-resistance standard thermometer, the circuit of Figure 1 exhibits ±2°C error over −40 to +125°C.

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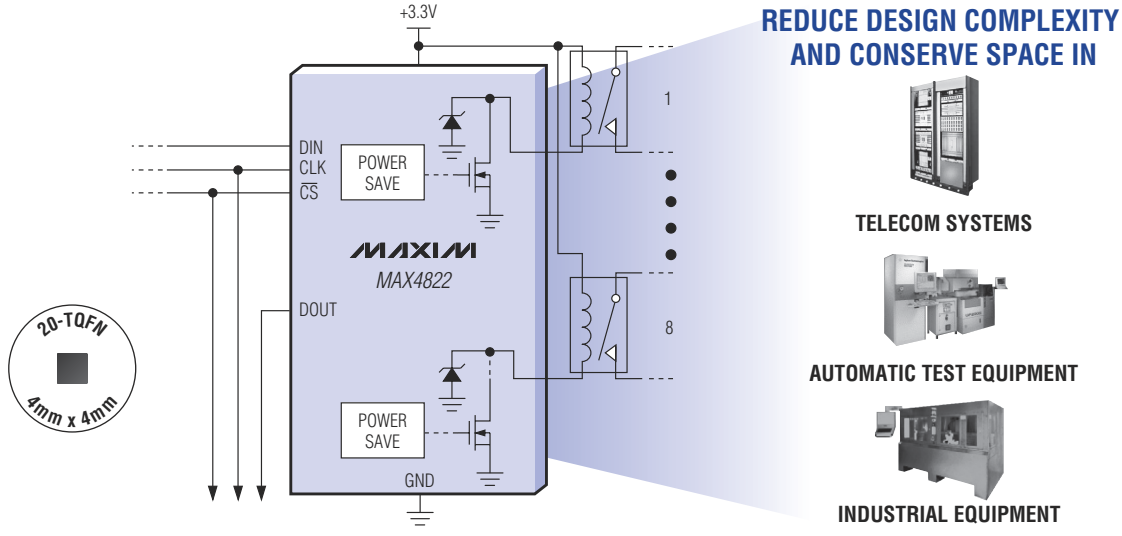

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MAX4822	8	4	SPI	3.3/5.0	Yes	Yes	20-TQFN (4 x 4)
MAX4823	8	4	SPI	3.3/5.0	No	Yes	20-TQFN (4 x 4)
MAX4824	8	4	Parallel	3.3/5.0	Yes	Yes	20-TQFN (4 x 4)
MAX4825	8	4	Parallel	3.3/5.0	No	Yes	20-TQFN (4 x 4)

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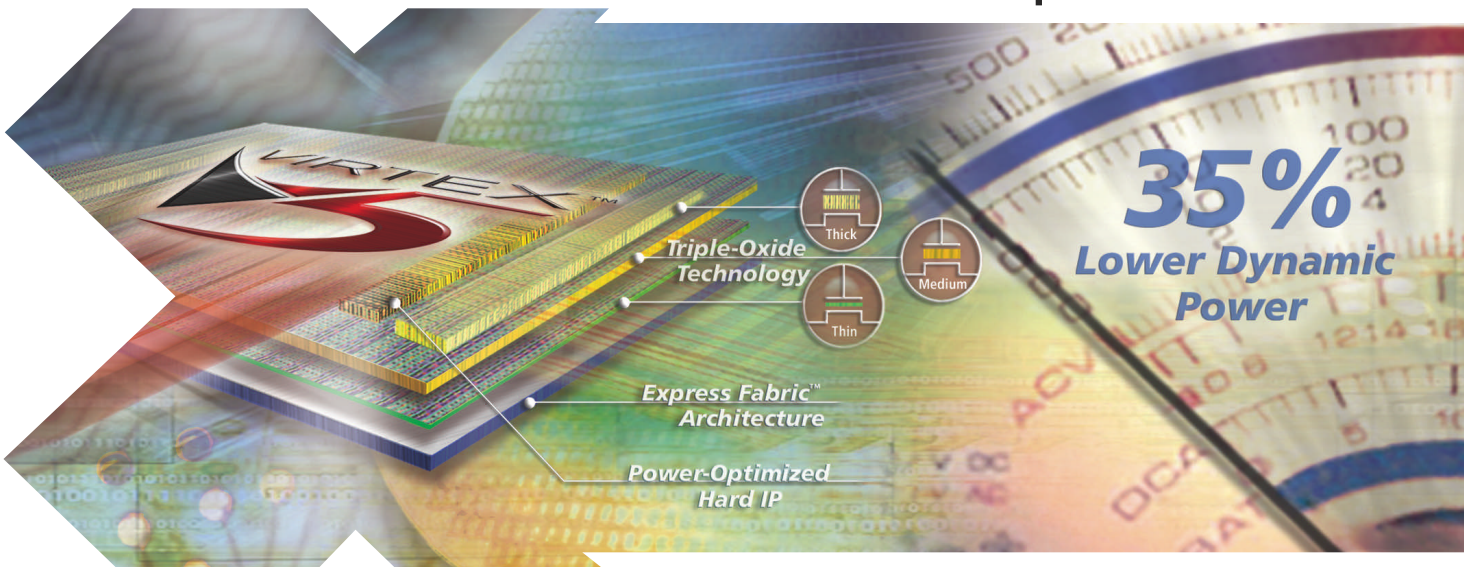

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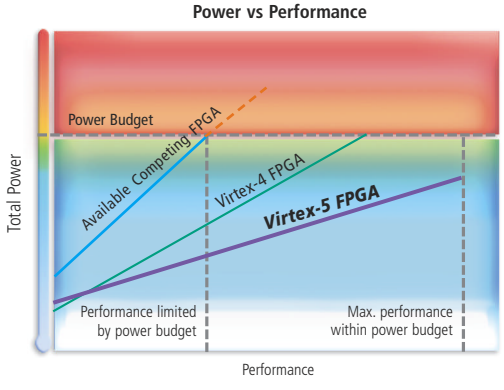

Note: Under worst-case operating conditions (85°C)

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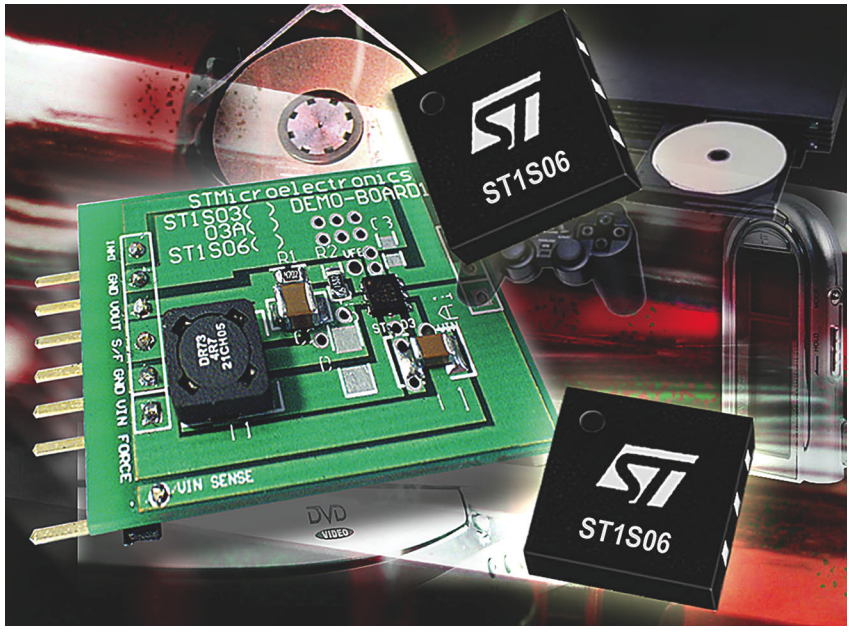

Voltage regulator requires few external components

Using a synchronous-rectification block instead of an external Schottky diode for 95% efficiency, the ST1S06 high-frequency, step-down, dc/dc converter has a 1.5A maximum-output-current capability and a 1.5-MHz switching frequency. Requiring a small inductor, two capacitors, and two resistors, the converter needs fewer external components than previous models. Providing a soft-start to prevent inrush current allows the device to minimize the start-up problems typical of battery-powered devices. The device is available in fixed-output voltages and in an adjustable version that uses an external resistor diode. It generates an adjustable output voltage from a 0.8V feedback voltage. The ST1S06 costs 35 to 45 cents (high volumes).

STMicroelectronics, www.st.com

Triple-output power switcher features medical-safety certifications

Accepting a universal input voltage of 90 to 264V dc or 127 to 300V dc and a frequency of 47 to 440 Hz, the triple-output, 50W LPT50 switching-power-supply series provides 3.3 to 24V of dc positive outputs, depending on the model. Measuring 2×4 in., the devices provide convection cooling and offer a 5.5W/in.^{3} rating.

The device can deliver 9A from the primary output. Also available with medical-safety certifications, the LPT50 costs $28.

Astec Power, www.astecpower.com

Three-chip-set reference designs are customizable online

Expanding on the vendor's myPower Online Design, the Powir+ chip-set reference designs and Web tools simplify and accelerate power-management-circuit design. Accelerating the design process by eliminating the need for design iterations, the IRPP3637-06A, IRPP3637-12A, and IRPP3637-18A reference designs come in 6, 12, and 18A power levels. Users can also modify standard designs on the vendor's Web site to create custom circuits. Each reference design comes with a suite of online simulation tools with small- and large-signal analysis, switching waveforms, and performance analysis for all components. The IRPP3637-06A targets low-current applications requiring reduced size and component count, using the vendor's IRF8910PbF dual SO-8 MOSFET. The IRPP3637-12A suits medium-current applications, using the vendor's IRF7823PbF and IRF832ZPbF independent SO-8 MOSFET and improving electrical and thermal efficiency. The IRPP3637-18A aims at medium- to high-current applications demanding high thermal performance, using the vendor's IRLR8713PbF and IRLR7843PbF D-Pak MOSFETS. The standard IRPP3637-xxA reference designs cost $150, and the customized IRPP3637-xxA reference designs cost $250.

International Rectifier, www.irf.com

Synchronous-buck regulator provides four output-voltage options

Targeting portable-system applications using lithium-ion batteries, the 1A SC194A synchronous-buck regulator has a 2.7 to 5.5V input-voltage range. The device includes a 17-µA quiescent current, 93% efficiency, a power-save mode, and protection features. Two programming pins allow users to set a 1, 1.2, 1.5, or 1.8V output voltage. Users can hard-wire them to set a constant voltage or tie them to a microcontroller and dynamically switch them for applications using digital-power control. Additional features include an internal compensation

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network and integrated switching FETs. The devices need no external Schottky diode. The SC194A costs $1.42 (1000).
Semtech, www.semtech.com

SMBus battery charger suits lithium-ion and nickel-chemistry batteries

Operating with or without a microcontroller, the LTC4101 precision smart-battery-charger controller complies with Revision 1.1 of the SMBus standard and meets SBS (Smart Battery System) Level 2 charging-function requirements. The charger suits 3 to 5.5V charging voltages for one-cell lithium-ion and three- to four-cell nickel-chemistry batteries. Capable of fast charging 4A with 0.8% voltage accuracy and 4% current accuracy, the device also features synchronous switching and provides high-efficiency charging from a 6 to 28V-wide input-supply-voltage range. Available in an SSOP-24 housing, the LTC-4101 costs $5 (1000).
Linear Technology, www.linear.com

Converter series provides three input-voltage ranges

The rugged IEXR and IEHR dc/dc-converter series comes in 10 to 16V-, 21 to 60V-, or 60 to 132V-dc ranges. The devices deliver 70 to 150W of output power; single-output-voltage models range from 8 to 52V dc, and two models have a 110V-dc output. Custom output voltages are also available. These convention-cooled converters come in a chassis-mount, vented enclosure with a 0 to 50°C temperature range with derating higher than 40°C. Available with 19-in.×2U rack mounting, or DIN-rail mounting, the IEXR and IEHR series cost $171 (100).
Schaefer, www.schaeferpower.com

Power supplies meet military standard 810E

The configurable NV-175 and NV-350 power-supply families meet the military 810E standards for shock, transit drop, bench handling, basic transportation, and shipboard vibration. The NV-175 comes with one to four outputs with a 3×5-in. footprint and cover and internal-fan options. The NV-350 delivers as many as six outputs and mounts in a 1U chassis. The NV series costs $89 (100) for a single-output, 180W configuration.
Lambda, www.lambdapower.com

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Development kit includes a single-board computer, software

Based on the 32-bit AVR32-based AP7000 DSC (digital-signal-controller) family, the "program-and-go" STK1000 development kit targets POS (point-of-sale), navigation, SOHO (small-office/home-office) network-gateway/router, and printer applications. Features include a production-ready, AVR32 single-board computer with an AT32AP7000 SOC (system on chip); a 3.5-in. TFT (thin-film-transistor) LCD; an audio DAC; and connectors for VGA, Ethernet USB, CompactFlash, and SD cards. The AT32AP7000 controller includes a vector-multiplication coprocessor, a 16-bit stereo-audio DAC, a 2048×2048 pixel TFT/STN (super-twist-nematic) LCD controller, a 480-Mbps USB 2.0 with on-chip transceivers, and two 10/100 Ethernet MACs (media-access controllers). Serial interfaces include RS-232, USART, I^2S, AC97, TWI (two-way interface)/I^2C, SPI, PS/2, and several SSCs (synchronous serial modules). Software for the development kit includes the Linux operating system; a GCC (GNU C compiler); a GNU debugger; all drivers, utilities, editors, and image viewers; and an IAR embedded workbench for AVR32. Application-ready C/C++ application software includes Web, FTP, and Telnet servers, in addition to utilities and libraries for video, sound, and displaying images. The STK1000 development kit costs $499. Providing emulations, the JTAGICE mkII is available separately for $299.
Atmel, www.atmel.com

RTOS occupies 10 kbytes in minimal configuration

Targeting the StarCore SC1000 and the SC2000 DSP-core families, the OSEck RTOS requires less than 10 kbytes of memory in a minimal configuration, suiting mobile-multimedia applications. The device delivers fully pre-emptive, event-driven, real-time response with a 300-nsec context-switch-

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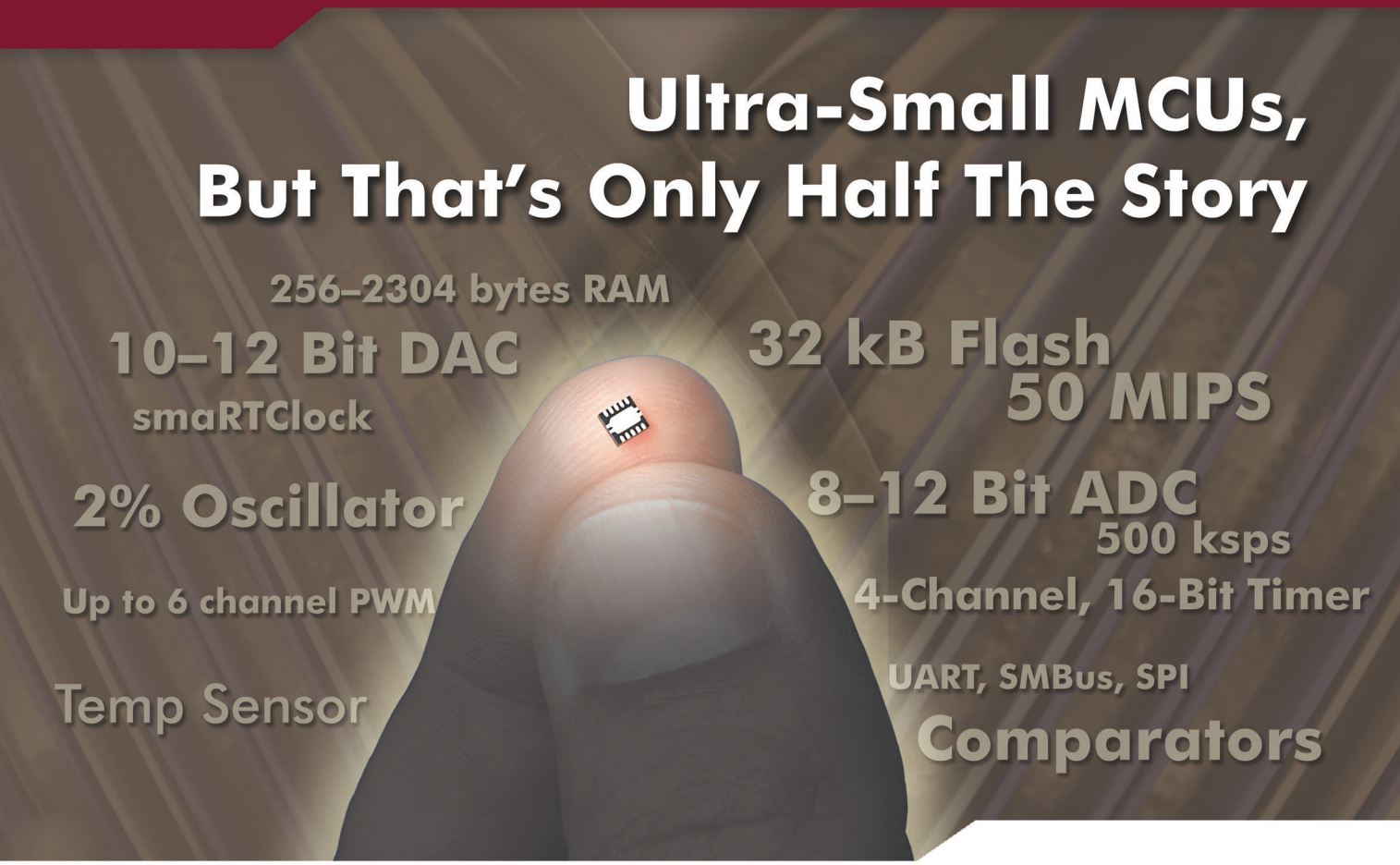

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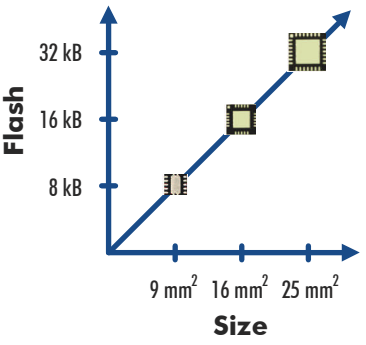

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ing speed and a 500-nsec worst-case interrupt latency. Additional features include built-in error detection and handling, and message-based Linx IPC (interprocess-communications) services. Developmental support for the platforms includes an RTOS-aware source-level debugger that supports freeze-mode debugging and postmortem analysis as well as a high-level run-mode-analysis tool that enables designers to study system details, including process/task information, CPU and memory profiling, task switching, and stack and memory usage. A single-seat SC1000 or SC2000 OSEck developers license costs $8000.

Enea, www.enea.com

Evaluation board includes a microcontroller-development kit

The MCBSTR9 evaluation board features the STR912FW-44X ARM966E-S-based microcontroller. Features include dual serial ports, a CAN (controller-area-network) interface, an SD-memory-card connector, an Ethernet interface, and eight LEDs. A USB interface provides board power, and a potentiometer allows analog-voltage input. A prototyping area allows developers to add their own hardware. The device comes with a microcontroller-development kit featuring ARM RealView compilation tools and the vendor's µVision debugger/simulator.

Keil, www.keil.com

POE controller features integrated diode bridges

Integrating on-chip diode bridges, a transient-surge protector, and a switching-regulator FET, the Si3400 POE (power-over-Ethernet) controller features IEEE 802.3af compliance. The diode bridges enable a proprietary early power-loss indicator as well as allow a direct connection to the RJ-45 connector. A PD (power-device) interface allows for programmable classification- and detection-signature circuitry; a switching-regulator controller; a dual current-limited hot-swap switch; and comprehensive protection circuitry, including a thermal-shutdown capability and support for nonisolated and isolated applications. Available in an ROHS (reduction-of-hazardous-substance)-compliant, 5×5 QFN-20, the device targets 802.3af-compliant PSE (power-sourcing equipment) and prestandard legacy PSE not compliant with the standard's inrush-current limits. The Si3400 costs $2.48 (10,000) with an available engineering-evaluation board and an Ethernet-system evaluation kit.

Silicon Laboratories, www.silabs.com

Microcontrollers feature an LCD controller for WVGA-sized screens

The 32-bit, 200-MHz SuperH microcontrollers feature an SH-2A CPU core with a built-in FPU (floating-point unit), an integrated CD-ROM decoder, and support for DRM (digital rights management) for audio content. The vendor claims a higher level of integration with these microcontrollers, integrating a host interface that supports USB 2.0 specifications and a display controller that supports color liquid-crystal panels as high as WVGA size at 800×480 pixels. The instruction set of the SH2A-FPU in the SH7263 and the SH7203 devices is upward-compatible with those of the SH-2A and SH-2 CPU cores; however, the vendor claims a 75% ROM-code-efficiency improvement compared with the SH-2 core. The SH7263 features an SRC (sampling-rate converter) that converts the audio-data-sampling frequency, an SSI (serial-sound interface) for input and output of digital-audio data, a serial-communication interface with a 16-

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MICROPROCESSORS

stage FIFO, and an I²C-bus interface. The device also includes an eight-channel, 10-bit ADC; a two-channel, 8-bit DAC; an eight-channel DMAC (direct-memory-access controller); a CAN (control-area-network) controller; and a NAND flash controller. A five-channel MTU2 (multifunction-timer unit) suits motor control and can produce a three-phase PWM (pulse-width-modulation)-wave output for controlling ac motors. The USB-powered E10A-USB requires no external power supply and suits use as an emulator. The SH7263 price ranges from $16.90 to $19.60.

Renesas Technology, www.renesas.com

INTEGRATED CIRCUITS

Analyzer displays results using sine-wave graphs

Measuring the amplitude, phase, and impedance responses of electronic, electro-acoustic, and other systems, the 10-Hz to 4-MHz C60 impedance and frequency-response analyzer displays results using a graphing program. This portable scientific test-and-measurement device tests the networks with a sine-wave excitation, displaying the results on a PC. Powered by a USB connection, the C60 costs $2800.

Cypher Instruments, www.cypherinstruments.co.uk

Triple-channel AFE IC provides low jitter

The triple-channel ISL98001 8-bit video AFE (analog-front-end) IC features the required functions for digitizing YPbPr video signals and RGB graphics signals from DVD players, VCRs, set-top boxes, and PCs. Suiting a variety of video resolutions, the device is available in five speeds, ranging from 140M to 275M pixels/sec. A fast conversion rate provides support for HDTV resolution as high as 1080 pixels and computer-monitor resolutions as high as QXGA. The digital phase-locked-loop technology provides a 450-psec maximum jitter (250 psec typical) peak to peak. Additional features include a peaking function, which compensates for input degradation during low-channel bandwidth, and integrated HSYNC and SOG signal processing, which eliminates the need for external sync slicers, sync separators, Schmitt triggers, and noise filters. Available in an MQFP-128 package, the ISL98001 costs $10.06 (1000).

Intersil, www.intersil.com

Digital temperature sensor targets low-power systems

Operating on a 1.7 to 3.7V supply-voltage range, the DS75LV digital temperature sensor targets low-power and battery-operated systems. The device is factory-calibrated to a ±2°C accuracy over its voltage-supply range at a −25 to +100°C temperature range and is ±3°C accurate over −55 to +125°C. A thermometer provides user-selectable 9-, 10-, 11-, and 12-bit digital temperature readings, translating to resolutions of 0.5°C for the 9-bit readings to 0.0625°C for the 12-bit readings. The thermostat function with user-defined trip points allows for a customizable threshold temperature and output hysteresis. A low-power shutdown mode is also available, reducing current draw to less than 2 µA. The DS75LV costs 90 cents (1000).

Dallas Semiconductor, www.maxim-ic.com

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scope

CHART YOUR COURSE

LOOKING AHEAD

The annual event for engineers who find their challenges below 25 kHz, the AES Audio Engineering Society Convention comes to San Francisco this year on Oct 5 to 8. A three-day product exhibition accompanies the four days of paper sessions and tutorials all at the Moscone Center. Now that the forefront of audio engineering encompasses not only audiophile products with envelope-pushing specifications but also an exploding cornucopia of mobile and desktop devices, the scope of the convention and the range of its appeal promise to be even broader than in the past. This is, amazingly, the 121st AES Convention, surely making it one of the longest running events on the electronics calendar.

LOOKING BACK

News extra:

Video-phone developed by Bell Labs uses existing telephone wires

NEW YORK, N.Y.—A TELEPHONE THAT TRANSMITS PICTURES TOGETHER WITH SOUNDS USING EXISTING TELEPHONE WIRES HAS BEEN DEVELOPED BY BELL TELEPHONE LABORATORIES. . . . THE VIDEO-PHONE DIFFERS FROM COMMERCIAL TELEVISION IN THAT IT SENDS SMALLER AND LESS DETAILED PICTURES EVERY TWO SEC. (*EDN*, September 1956)

LOOKING AROUND

What's that about a downturn?

As we approach the fourth quarter, forecasters have been quietly backing off from their semiconductor-industry-growth projections for 2006. The consensus seems to be that the year will come in somewhere from 5 to 8% higher than 2005—not a disaster, but nothing to make executives pull out their checkbooks, either. Beneath those numbers, though, there's important detail, according to iSuppli principal analyst Gary Grandbois. DRAM shipments dominate the top-line numbers, and DRAM is tied to a few specific kinds of products, such as PCs. As it happens, PCs have not had a good 2006. Sales are soft, and the mix is shifting from desktops to notebooks. Cellular handsets and consumer devices—which represent a lot more design starts than PCs—have done pretty well. So a soft top line is not necessarily bad news for the design community.

OrCAD PCB Designer has a growing number of fans

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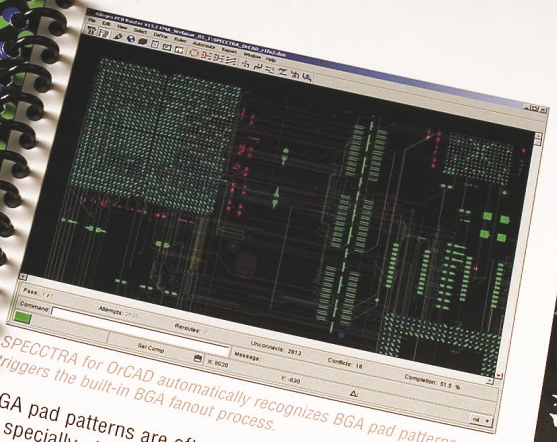
Design Solution #9

How do I fanout high-pin-count and metric BGAs?



SPECCTRA for OrCAD automatically recognizes BGA pad patterns and triggers the built-in BGA fanout process.

BGA pad patterns are often defined and located on metric or specially pitched spacing that are at odds with a user's grid settings. SPECCTRA® for OrCAD centers BGA fanout vias between the surface mount distribution pads automatically. Users don't need to calculate or set special grid settings. The correct, centered via location is computed regardless of whether the BGA is metric or mils. SPECCTRA for OrCAD recognizes BGA pad patterns and automatically triggers its powerful built-in BGA fanout process. No special commands are required to create successful BGA fanout. The BGA PADS are fanned out with dogbone-style vias directed diagonally to the four corners of the BGA to create wide power-feed channels to the BGA interior. Widths associated with each net are recognized during BGA fanout. When the BGA is fanned out, the wider net widths for the power and ground nets are used to fanout to the power planes.

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- *Easy-to-use PSoC tools provide system-level embedded design with quick time-to-market*

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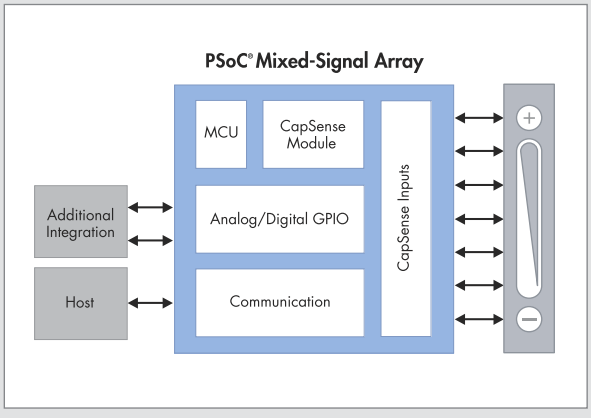
CYPRESS CAPSENSE CIRCUIT DIAGRAM



PSoC® CapSense implementation with two buttons and a slider using a single PSoC device.

CapSense Device Selector Guide

Device	Resources	Available Package
CY8C21x34	8 KB Flash, 512 B RAM, I²C, SPI	16-SOIC, 20-SSOP, 28-SSOP, 5x5 mm 32-MLF
CY8C24x94	16 KB Flash, 1 KB RAM, I²C, Full-speed USB, SPI	8x8 mm 56-MLF

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